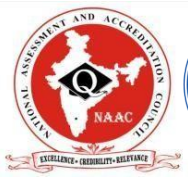
QMP 7.1 D/F

Channabasaveshwara Institute of Technology



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NH 206 (B.H. Road), Gubbi, Tumkur – 572 216. Karnataka

Department of Electronics & Communication Engineering

Electronic Principles and circuits – BEC303

B.E - III Semester

Lab Manual 2024-25

Name : _____

USN : _____

Batch : _____ Section : _____

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Electronic Principles and circuits – BEC303

Prepared & Reviewed by:

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Assistant Professor

Approved by:

Dr.Thejaswini R
Professor & Head,Dept. of ECE

INSTITUTE VISION

To create centres of excellence in education and to serve the society by enhancing the quality of life through value based professional leadership.

INSTITUTE MISSION

- To provide high quality technical and professionally relevant education in a diverse learning environment.
- To provide the values that prepare students to lead their lives with personal integrity, professional ethics and civic responsibility in a global society.
- To prepare the next generation of skilled professionals to successfully compete in the diverse global market.
- To promote a campus environment that welcomes and honors women and men of all races, creeds and cultures, values and intellectual curiosity, pursuit of knowledge and academic integrity and freedom.
- To offer a wide variety of off-campus education and training programmes to individuals and groups.
- To stimulate collaborative efforts with industry, universities, government and professional societies.
- To facilitate public understanding of technical issues and achieve excellence in the operations of the institute.

QUALITY POLICY

Our organization delights customers (students, parents and society) by providing value added quality education to meet the national and international requirements. We also provide necessary steps to train the students for placement and continue to improve our methods of education to the students through effective quality management system, quality policy and quality objectives.

Vision

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

To create globally competent Electronics and Communication Engineering

Mission

professionals with ethical and moral values for the betterment of the society

- To nurture the technical/professional/engineering and entrepreneurial skills for overall self and societal upliftment through co-curricular and extra-curricular events.
- To orient the Faculty/Student community towards the higher education, research and development activities.
- To create the Centres of Excellence in the field of electronics and communication in collaboration with industries/Universities by training the faculty through latest technologies.
- To impart quality technical education in the field of electronics and communication engineering to meet over the current/future global industry requirements.

Program Educational Objectives (PEO's)

After four Years of Graduation, our graduates are able to:

- Provide technical solutions to real world problems in the areas of electronicsand communication by developing suitable systems.
- Pursue engineering career in Industry and/or pursue higher education andresearch.
- Acquire and follow best professional and ethical practices in Industry andSociety.
- Communicate effectively and have the ability to work in team and to lead theteam.

Program Specific Outcomes (PSO's)

At the time of graduation, our graduates are able to:

PSO1: Specify, design, build and test analog and digital systems for signal processing including multimedia applications, using suitable components or Simulation tools.

PSO2: Understand and architect wired and wireless analog and digital Communication systems as per specifications and determine their performance.

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Karnataka

DEPARTMENT OF ELECTRONICS & COMMUNICATIONENGINEERING

SYLLABUS

Course Code:	BEC303	**CIE Marks:**	25
Lab Duration:	2 hours		
Laboratory Experiments		**RBT Level**	
1. Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener Voltage Regulator		L3	
2. Design and Test Biased Clippers – a) Positive, b) Negative, c) Positive-Negative Positive and Negative Clampers with and without Reference		L3	
3. Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.		L3	
4. Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely: drain resistance, mutual conductance and amplification factor.		L3	
5. Design and Test (i) Emitter follower, (ii) Darlington connection		L3	
6. Design and plot the frequency response of Common Source JFET/MOSFET amplifier.		L3	
7. Test the Op-amp comparator with zero and non-zero reference and obtain the Hysteresis curve.		L3	
8. Design and test Full-wave controlled rectifier using RC triggering circuit.		L3	
9. Design and test Precision Half wave and Full wave rectifiers using Op-amp.		L3	
10. Design and test RC phase shift oscillator.		L3	

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Karnataka

Department of Electronics and Communication Engineering

Electronic Principles and circuits: Outcomes

COURSE OUTCOMES :

After completing this course the student could be able to:

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

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Department of Electronics and Communication Engineering

'Instructions to the Candidates'

- Student should come with thorough preparation for the experiment to be conducted.
- Student should take prior permission from the concerned faculty before availing the leave.
- Student should come with proper dress code and to be present on time in the laboratory.
- Student will not be permitted to attend the laboratory unless they bring the practical record fully completed in all respects pertaining to the experiment conducted in the previous class.
- Student will not be permitted to attend the laboratory unless they bring the observation book fully completed in all respects pertaining to the experiment to be conducted in present class.
- Experiment should be started conducting only after the staff-in-charge has checked the circuit diagram.
- All the calculations should be made in the observation book. Specimen calculations for one set of readings have to be shown in the practical record.
- Wherever graphs to be drawn, A-4 size graphs only should be used and the same should be firmly attached in the practical record.
- Practical record and observation book should be neatly maintained.
- Student should obtain the signature of the staff-in-charge in the observation book after completing each experiment.
- Theory related to each experiment should be written in the practical record before procedure in your own words with appropriate references.

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Sl. No	Name of the Experiment	Date			Manual Marks (Max . 20)	Record Marks (Max. 10)	Signature (Student)	Signature (Faculty)
		Conduction	Repetition	Submission of Record				
1	Design and Test (iii) Bridge Rectifier with Capacitor Input Filter (iv) Zener Voltage Regulator							
2	Design and Test Biased Clippers – a) Positive, b) Negative, c) Positive-Negative Positive and Negative Clampers with and without Reference							
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.							
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.							
5	Design and Test (i) Emitter follower, (ii) Darlington connection							
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier.							
7	Test the Op-amp comparator with zero and non-zero reference and obtain the							

	Hysteresis curve.							
8	Design and test Full-wave controlled rectifier using RC triggering circuit.							
9	Design and test Precision Half wave and Full wave rectifiers using Op-amp.							
10	Design and test RC phase shift oscillator.							
Average								

Experiment No.1

DESIGN AND TEST

i) Bridge Rectifier with Capacitor Input Filter

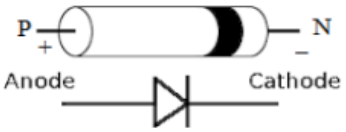
AIM:

To design and test a bridge rectifier with capacitor input filter and determine ripple factor.

APPARATUS REQUIRED:

Transformer (1), Diodes 1N4007 (4), Resistor 430 Ω (1), Capacitor 102μF (1), Breadboard and CRO.

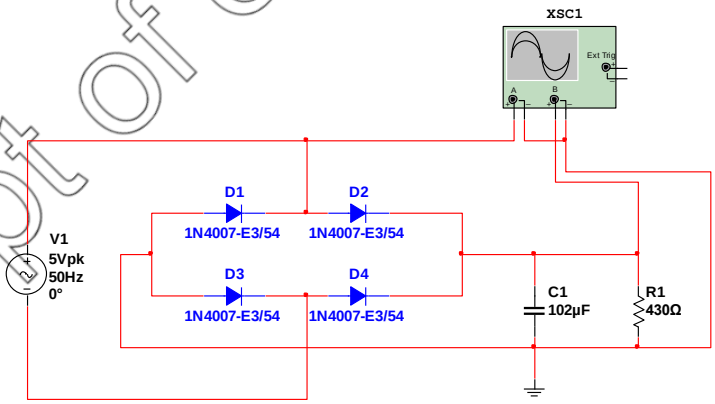
DIODE SYMBOL:



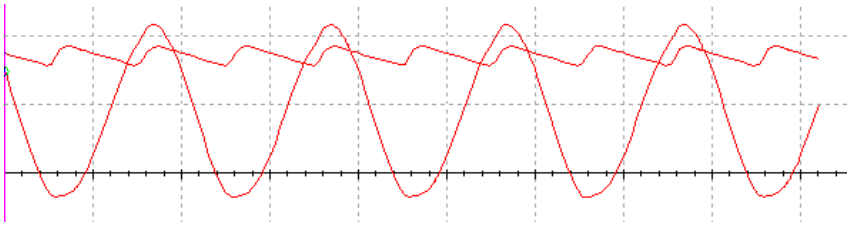
PROCEDURE

1. Make the connections as shown in the circuit diagram.
2. Apply AC input from the Mains and display the output on CRO.
3. Observe the output.

CIRCUIT DIAGRAM:



OUTPUT WAVEFORM:



RESULT

ii) Zener Voltage Regulator

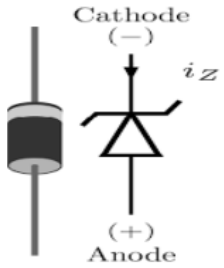
AIM:

To design and test a Zener voltage regulator to determine the line and load regulation characteristics.

APPARATUS REQUIRED:

Transistor SL 100, Resistor (220 Ω), Decade resistance box, Power supply, CRO, Zener diode (1N4736).

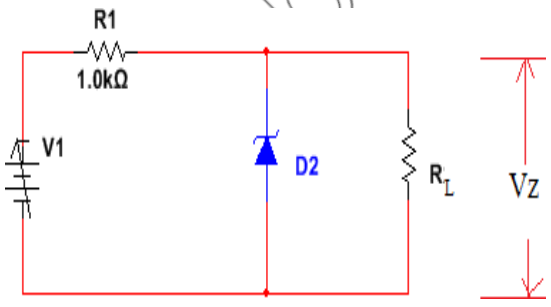
ZENER DIODE SYMBOL:



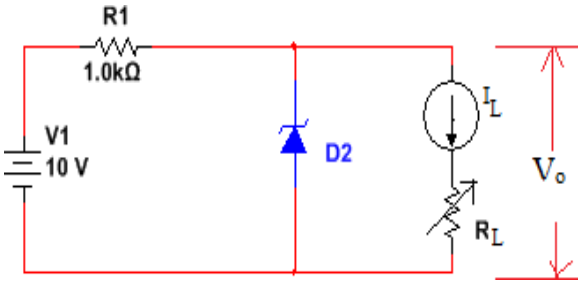
PROCEDURE:

1. Make the connections as shown in the figure.
2. Set the minimum voltage at the input above the Zener break down voltage.
3. For line regulation, vary the input supply and note down the output voltage.
4. For load regulation, vary the load resistance and note down the output voltage.
5. Calculate the % line and load regulation.

CIRCUIT DIAGRAM:



Line Regulation



Load Regulation

TABULAR COLUMN:

Line Regulation: R_L = 1 kΩ			**Load Regulation:** V_i = 15 V constant		
Sl. No.	V_i	V_o	Sl. No.	R_L	V_o
1			1		
2			2		
3			3		

RESULT:

V_{HL} = High line/Input DC voltage
V_{LL} = Low line/Input DC voltage

V_{NL} = DC output voltage at no load (open circuit)
V_{FL} = DC output voltage at full load (R_L = 1 kΩ)

% Line regulation = $(V_{HL} – V_{LL} / V_{LL}) \times 100$ = ……

% Load regulation = $(V_{NL} – V_{FL} / V_{FL}) \times 100$ = ……

Experiment No. 2

DESIGN AND TEST CLIPPER AND CLAMPER CIRCUITS

AIM:

To design clipper and clamper circuits for the given specification and hence to plot the output.

APPARATUS REQUIRED:

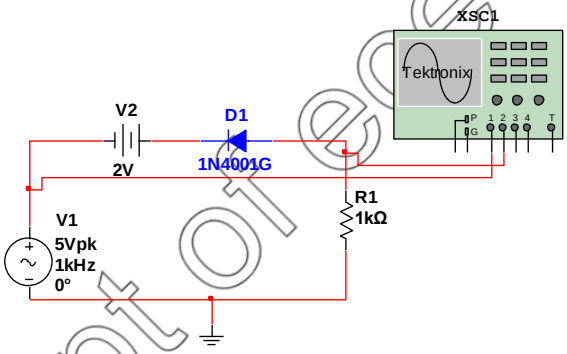
Diode iN4007 (2), Resistor 1 kΩ (1), Capacitor 1 μF (1), CRO, Probes, Breadboard, wires, Power supplies (0-30 V/2A) (2).

PROCEDURE:

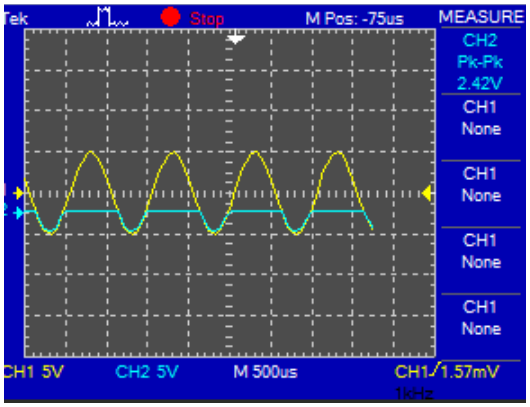
1. Make the connections as shown in the circuit diagram.
2. Apply sine wave for clippers and square wave for clampers whose amplitude is greater than the clipping and clamping level (Set $V_i = 10V_{p-p}$ and f = 1 kHz).
3. Observe the output waveform V_o in the CRO by keeping ac/dc switch to dc.

A) Biased Clippers

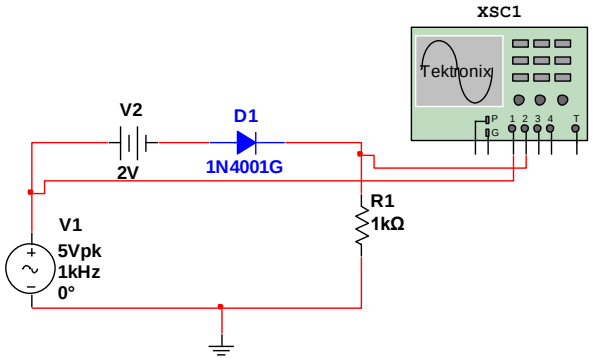
i) Positive Series Biased Clipper:



EXPECTED GRAPH:



ii) Negative Series Biased Clipper:



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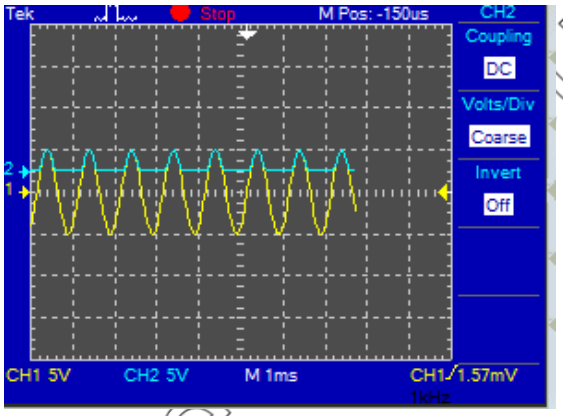
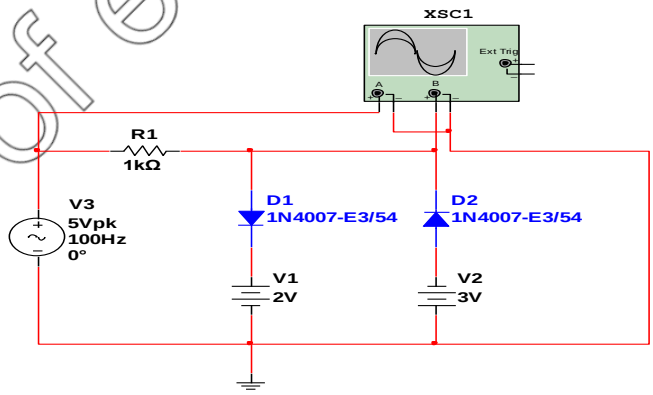
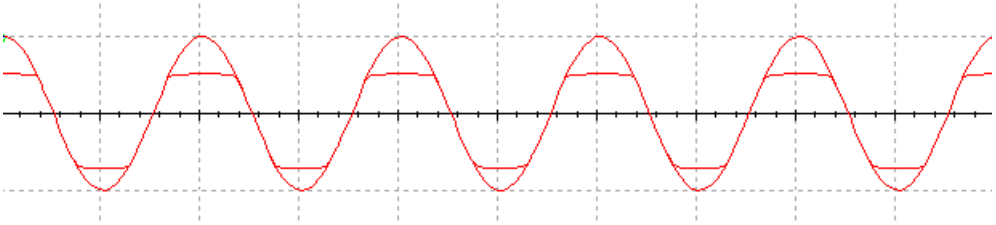


iii) Double Ended Clipper:

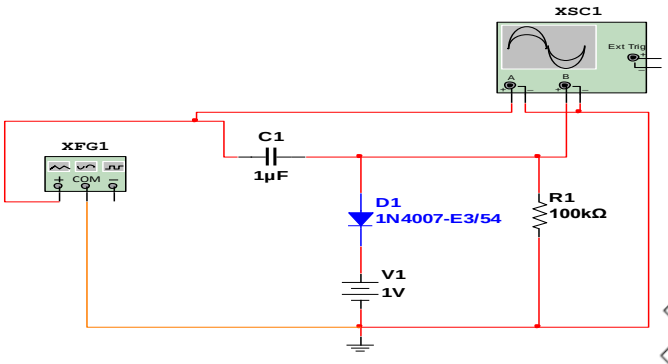


EXPECTED GRAPH:

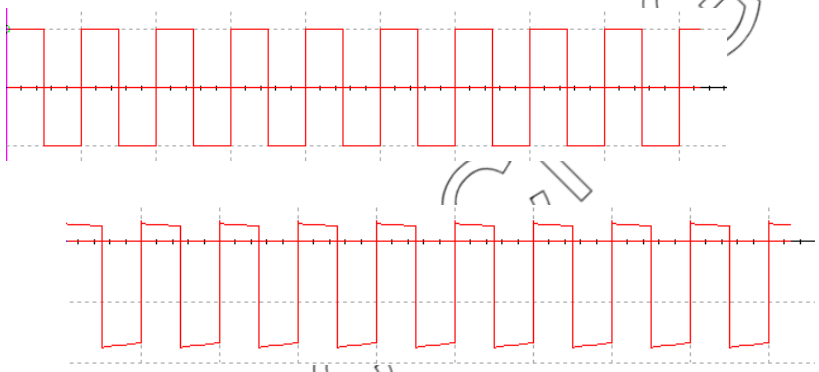


B) Clamper Circuits with Reference

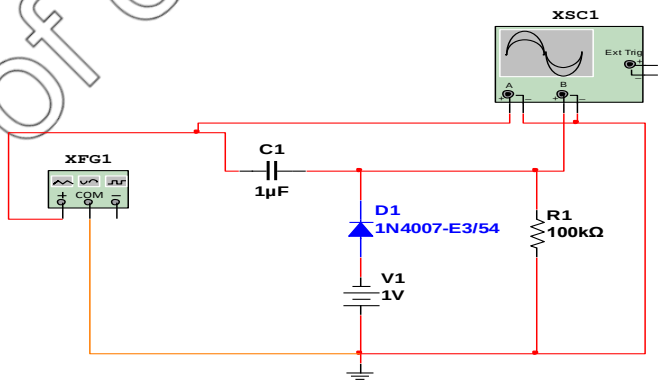
i) Negative Biased Clamper:



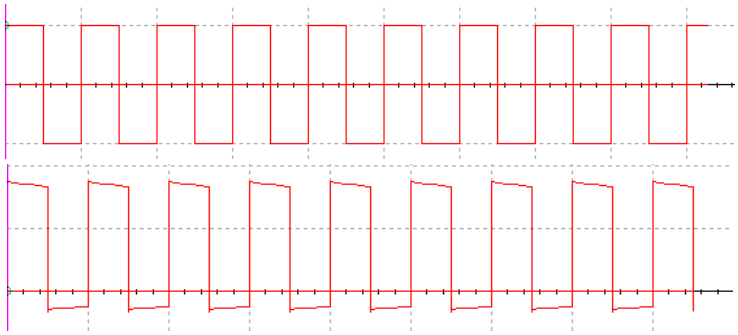
EXPECTED GRAPH:



ii) Positive Biased Clamper:

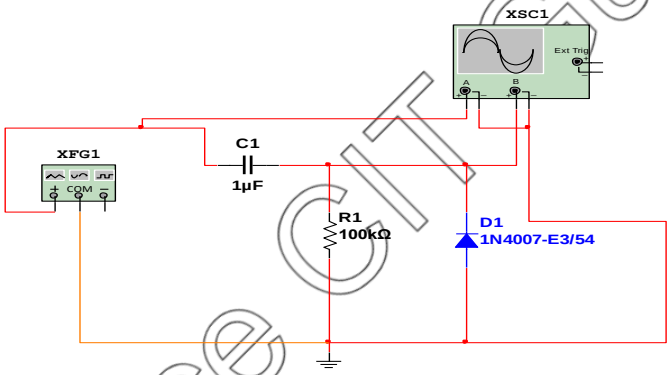


EXPECTED GRAPH:

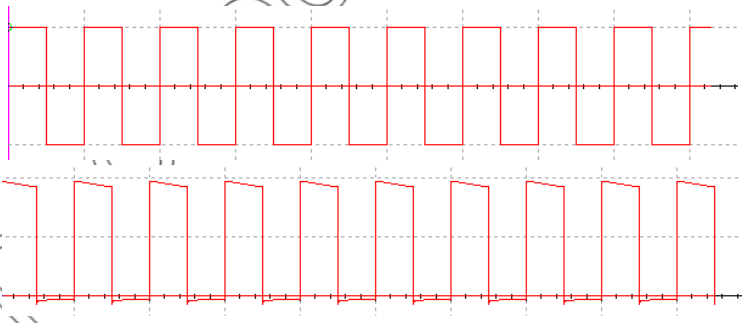


C) Clamper Circuits without Reference

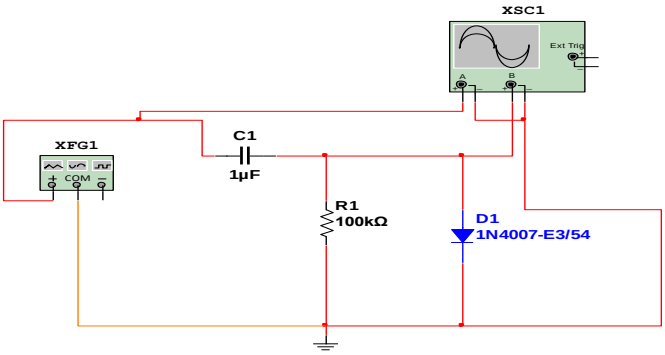
iii) Positive Clamper without reference:



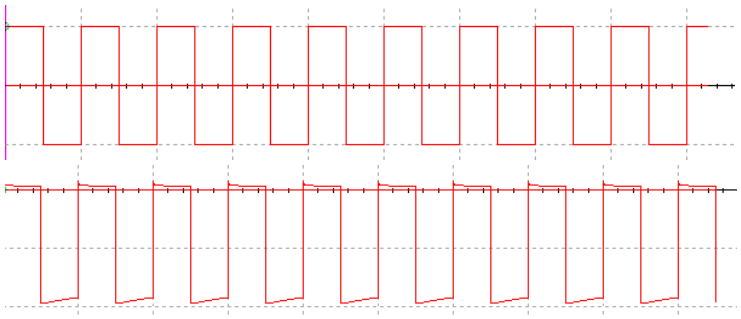
EXPECTED GRAPH:



iv) Negative Clamper without reference:



EXPECTED GRAPH:



RESULTS:

Experiment No. 3

CHARACTERISTICS OF JFET

AIM:

To plot the transfer and drain characteristics of JFET and calculate its drain resistance, mutual conductance and amplification factor.

APPARATUS REQUIRED:

Power supply (0-30)V, Ammeter (0-30)μA, Voltmeter (0-30)V, Bread board, wire, Transistor (NPN) and Resistors 1 kΩ (2).

PROCEDURE:

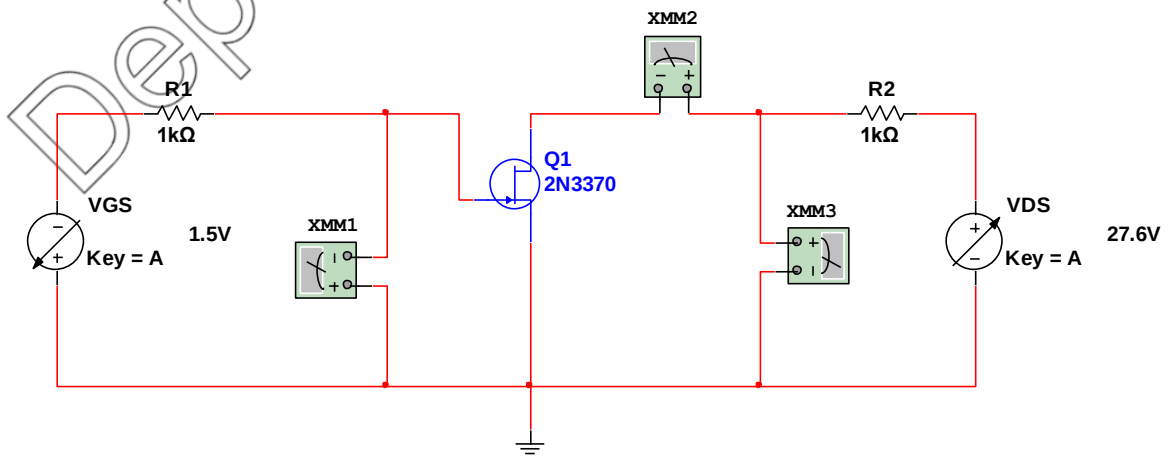
Drain Characteristics

1. Make the connections as shown in the circuit diagram.
2. Set V_{GS} and vary V_{DS} in steps of 0.5 V and note down the corresponding I_D.
3. Repeat step 2 for various values of V_{GS}.
4. Plot the graph: V_{DS} vs I_D for constant values of V_{GS}.
5. Find the drain resistance $R_d = \Delta V_{DS} / \Delta I_D$ with V_{GS} constant.

Transfer Characteristics

1. Make the connections as shown in the circuit diagram.
2. Set V_{DS} and vary V_{GS}in steps of 0.5 V and note down the corresponding I_D.
3. Repeat step 2 for various values of V_{DS}.
4. Plot the graph: V_{GS} vs I_D for constant values of V_{DS}.
5. Find the transconductance, $G_m = \Delta I_D / \Delta V_{GS}$ with V_{DS} constant.

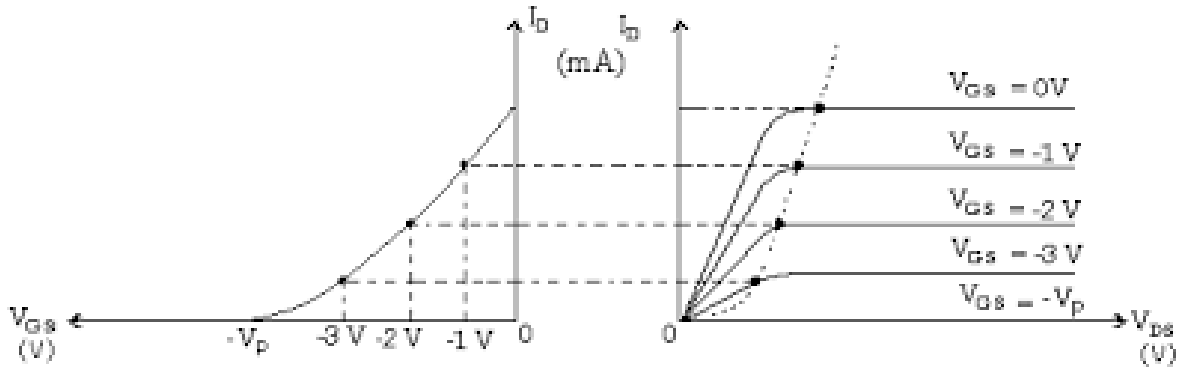
CIRCUIT DIAGRAM:



TABULAR COLUMN:

DRAIN CHARACTERISTICS				TRANSFER CHARACTERISTCS	
V_{GS} (V) =		V_{GS} (V) =		V_{DS} =	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

EXPECTED GRAPH:



CALCULATION:

Drain Characteristics $R_d = \Delta V_{DS} / \Delta I_D$, V_{GS} = constant

Mutual Conductance $G_m = \Delta I_D / \Delta V_{GS}$, V_{DS} = constant

Amplification factor $\mu = R_d * G_m$

RESULT:

Experiment No. 4

CHARACTERISTICS OF n-CHANNEL MOSFET

AIM:

To plot the transfer and drain characteristics of n-channel MOSFET and calculate its drain resistance, mutual conductance and amplification factor.

APPARATUS REQUIRED:

Power supply (0-30) V, Ammeter (0-100) mA, Voltmeter (0-30) V. Bread board and wires, Transistor.

PROCEDURE:

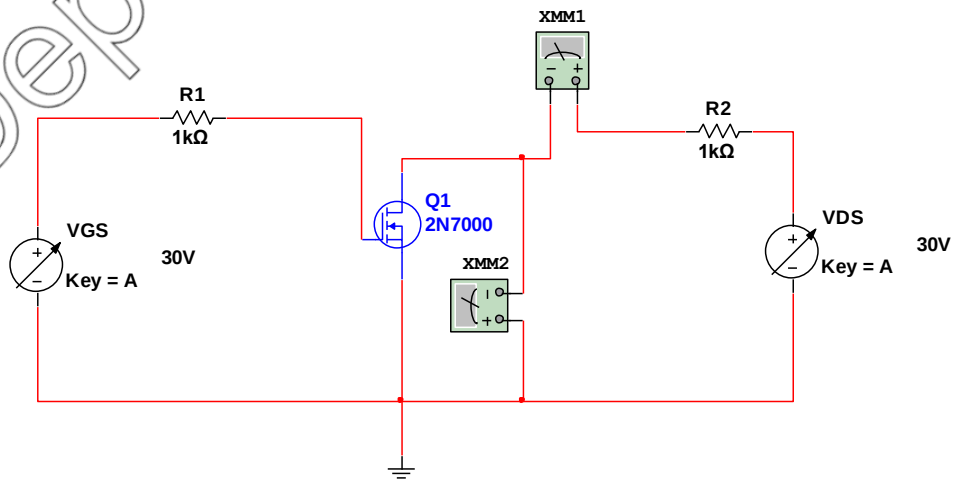
Drain Characteristics

1. Make the connections as shown in the circuit diagram.
2. Set V_{GS} = 0 V and vary V_{DS} in steps of 0.5 V and note down the corresponding I_D.
3. Repeat the above procedure for V_{GS} = -1, -2, -3 V, for the depletion mode.
4. Repeat the above procedure for V_{GS} = 1, 2, 3 V, for enhancement mode.
5. Plot the graph: V_{DS} vs I_D for constant values of V_{GS}.
6. Find the drain resistance $R_d = \Delta V_{DS} / \Delta I_D$ with V_{GS} constant.

Transfer Characteristics

1. Make the connections as shown.
2. Set V_{DS} and vary V_{GS} in steps of 0.5 V and note down the corresponding I_D.
3. Repeat the above procedure for various values of V_{DS}.
4. Plot the graph: V_{GS} vs I_D for constant values of V_{DS}.
5. Find the transconductance, $G_m = \Delta I_D / \Delta V_{GS}$ with V_{DS} constant.

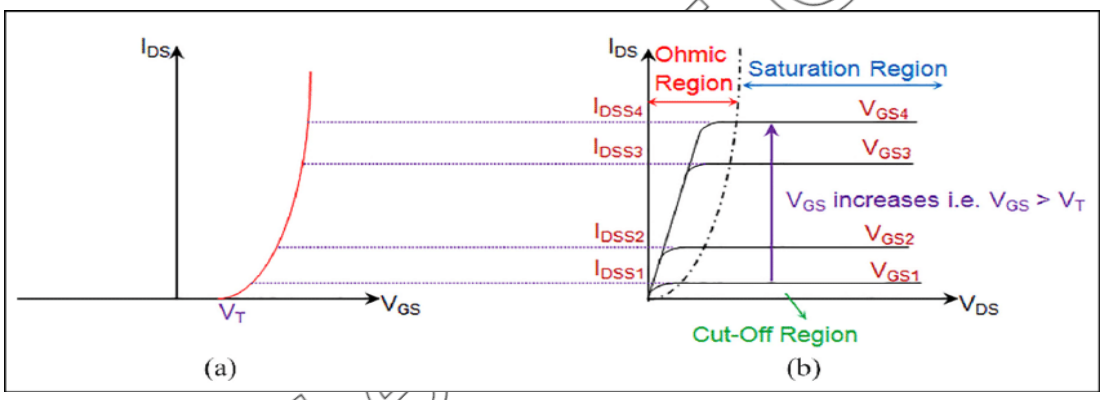
CIRCUIT DIAGRAM:



TABULAR COLUMN:

DRAIN CHARACTERISTICS				TRANSFER CHARACTERISTCS	
V_{GS} (V) =		V_{GS} (V) =		V_{DS} =	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

EXPECTED GRAPH:



CALCULATION:

Drain Characteristics $R_d = \Delta V_{DS} / \Delta I_D$, V_{GS} = constant

Mutual Conductance $G_m = \Delta I_D / \Delta V_{GS}$, V_{DS} = constant

Amplification factor $\mu = R_d * G_m$

RESULT:

Experiment No. 5

DESIGN AND TEST EMITTER FOLLOWER AND DARLINGTON CONNECTION

AIM:
To design and test the Emitter follower circuit and the Darlington connection.

APPARATUS REQUIRED:
Transistor NPN (2), Resistors, Capacitors, Power supply, CRO.

A) Emitter Follower:

DESIGN:
Let the Q point be (V_{ce}, I_c) = (5 V, 5 mA).
Let β = 100 and V_{cc} = 10 V.

R_E:
$V_{RE} = V_{CC}/10 = 10/10 = 1$ V
$I_E R_E = 1$ V
$R_E = 1/I_E = 1/I_C = 1/5\text{mA} = 200\ \Omega$ (Choose $R_E = 220\ \Omega$)

R_C:
Applying KVL in CE loop,
$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$
$I_C R_C = 10\text{-}5\text{-}1 = 4$
$R_C = 4/I_C = 4/5\text{mA} = 800\ \Omega$ (Choose $R_C = 820\ \Omega$)

R_1:
From the above biasing circuit,
$V_B = V_{BE} + V_{RE} = 0.7 + 1 = 1.7$ V
$I_C = \beta I_B$
$I_B = 50\mu A$
Assume $10I_B$ flows through R_1,
$R_1 = V_{CC} - V_B / 10I_B = (10\text{-}1.7)/(10 \times 50\mu A) = 16.6\ k\Omega$ (Choose $R_1 = 18\ k\Omega$)

R_2:
$R_2 = V_B/9I_B = 1.7/(9 \times 50\mu A) = 3.77\ k\Omega$ (Choose $R_2 = 4.7\ k\Omega$)

C_E:

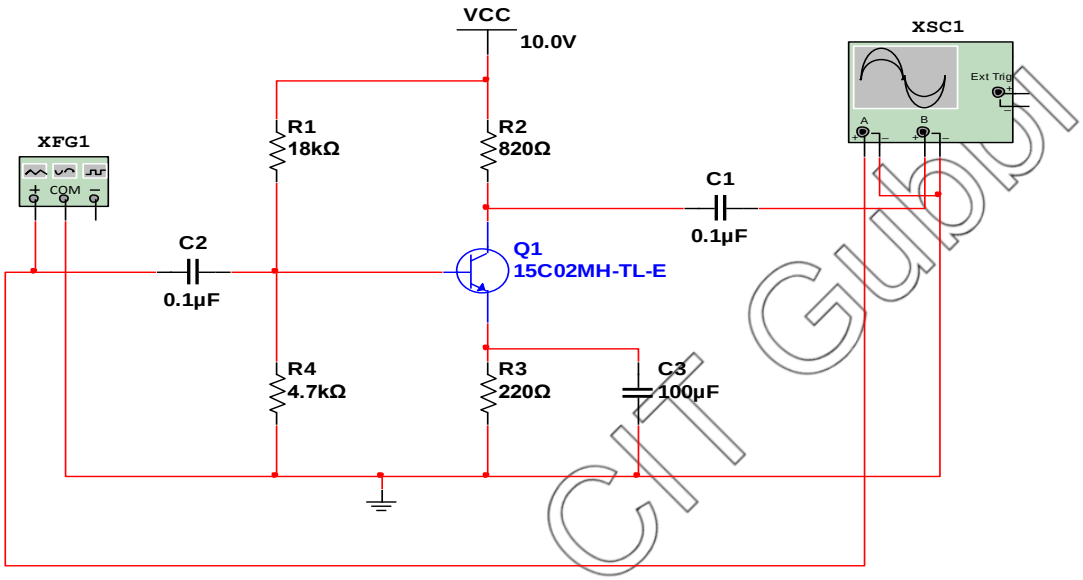
Let $X_{CE} = R_E/10$; $1/2\pi fC_E = R_E/10$

$C_E = 10/2\pi fR_E$

At f=100 kHz, C_E = 72.34 μF (Choose C_E = 100 μF)

Choose $C_1 = C_2$ = 0.1 μF

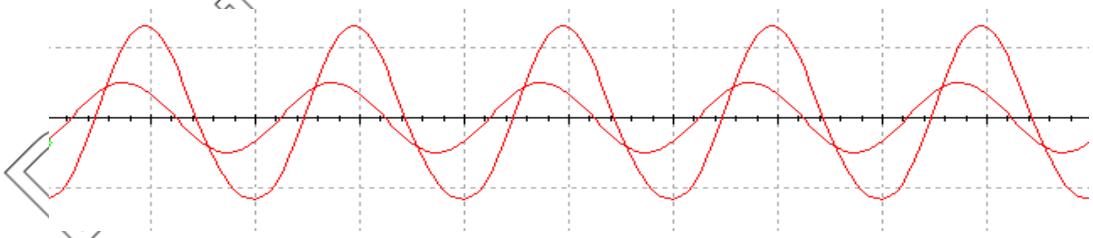
CIRCUIT DIAGRAM:



PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Keep the input signal amplitude slightly less than the maximum signal handling capacity.
3. Observe the output.

EXPECTED GRAPH:



RESULT:

B) Darlington Connection:

DESIGN:

Let V_{CC} = 12 V, $I_{C2} = I_{C1}$ = 5 mA = I_{E2}, β = 100.

Choose $V_{CE2} = V_{CC}/2$ = 6 V = $V_{E2} = I_E R_E$

R_E = 6/5mA = 1.2 kΩ

$V_{B1} = V_{BE1} + V_{BE2} + V_{E2}$ = 0.7 + 0.7 + 6 = 7.4 V

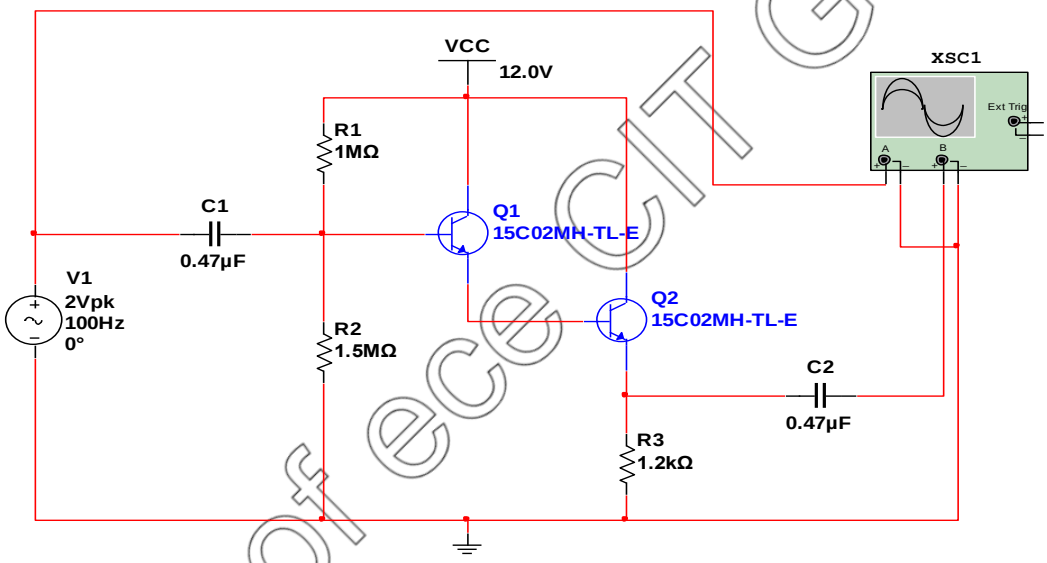
$I_{B2} = I_C/\beta = I_{B2}/\beta$ = 0.0005 mA

$V_{B1} = 7.4 = V_{CC}R_2/[R_1+R_2]$

Let R_2 = 1.5 MΩ. Calculating, we get R_1 = 932.4 kΩ (Choose 1 MΩ)

Assume $C_{C1} = C_{C2}$ = 0.47 μF

CIRCUIT DIAGRAM:



PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Apply a sinusoidal voltage of small amplitude (say 1 V).
3. Observe the output.

EXPECTED GRAPH:

RESULT:

Experiment No. 6

FREQUENCY RESPONSE OF COMMON SOURCE JFET/MOSFET AMPLIFIER

AIM:

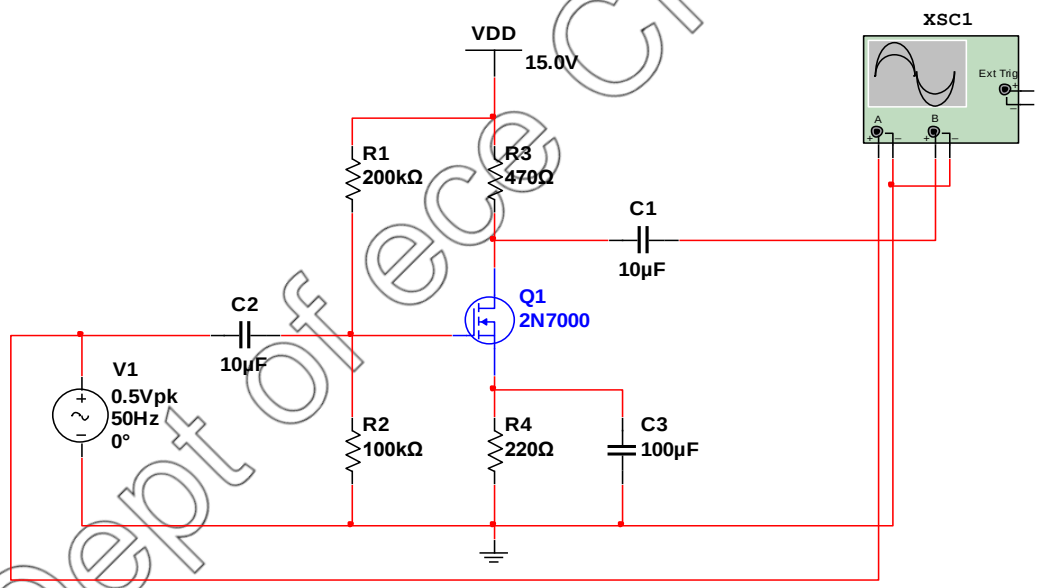
To obtain the frequency response of a common source JFET/MOSFET amplifier.

APPARATUS REQUIRED:

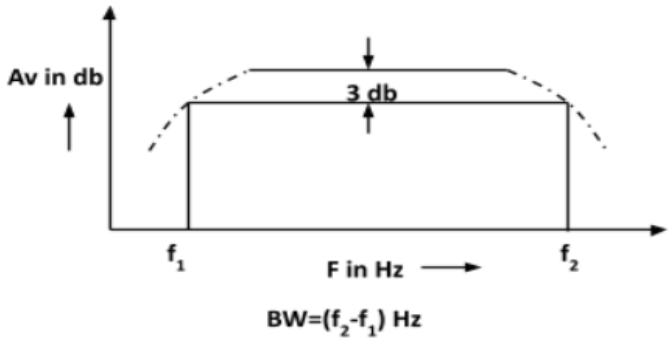
FET BFW 10, Resistors 2.2 MΩ, 1 kΩ, 2.7 kΩ, Capacitor 0.1 μF, 47 μF, Power supply, AFO, CRO.

PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Keep the input signal amplitude slightly less than maximum signal handling capacity. (Max signal handling capacity is the input voltage at which output gets clipped)
3. Vary the frequency and note down the output up to 1 MHz.
4. Plot the frequency response on semi log sheet.



Frequency Response:



TABULAR COLUMN:

Input voltage $V_{in(p\text{-}p)}$ = ……

Frequency (Hz)	Output (p-p) V	Voltage gain (V_o/V_i)	Gain = 20 log(V_o/V_i)

RESULT:

Experiment No. 7

COMPARATOR WITH ZERO AND NON-ZERO REFERENCE

AIM:

To design and test a comparator circuit with zero and non-zero reference using op-amp and to obtain the Hysteresis curve.

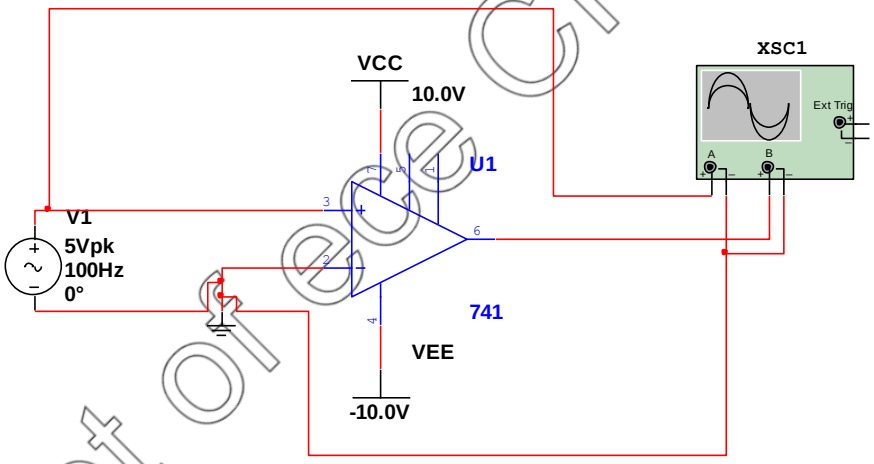
APPARATUS REQUIRED:

741 op-amp IC, Power supply, Resistors

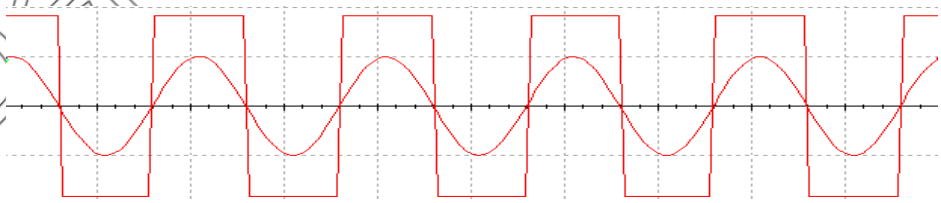
PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Set the input signal to sine wave with amplitude 1 V(p-p) and frequency 1 kHz.
3. Observe the output waveforms.

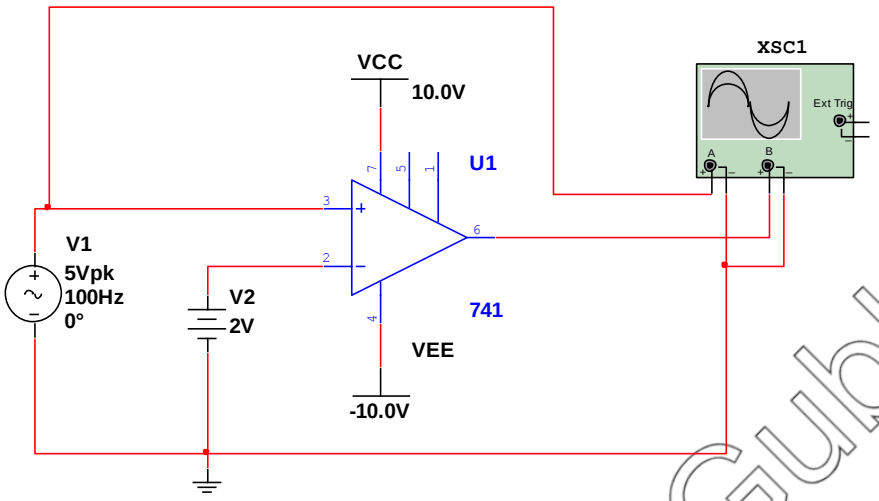
A) Comparator with zero reference:



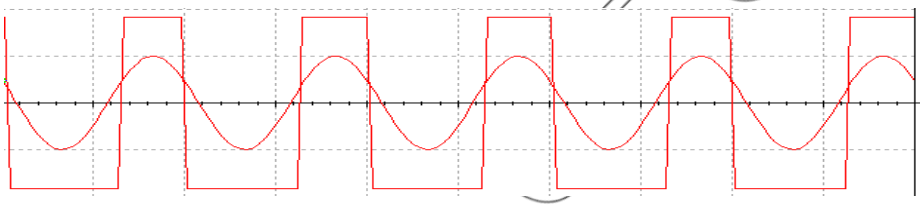
EXPECTED GRAPH:



B) Comparator with non-zero reference:



EXPECTED GRAPH:



C) Schmitt Trigger:

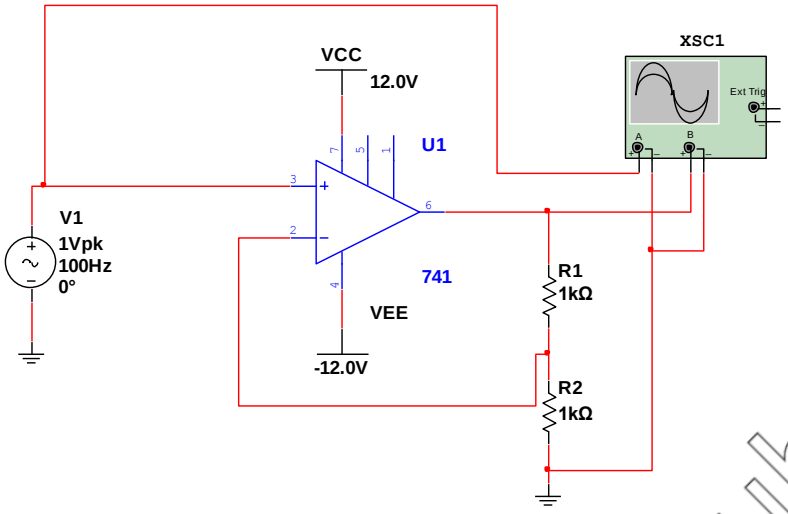
DESIGN:

Taking UTP = =6 V and LTP = -6 V.

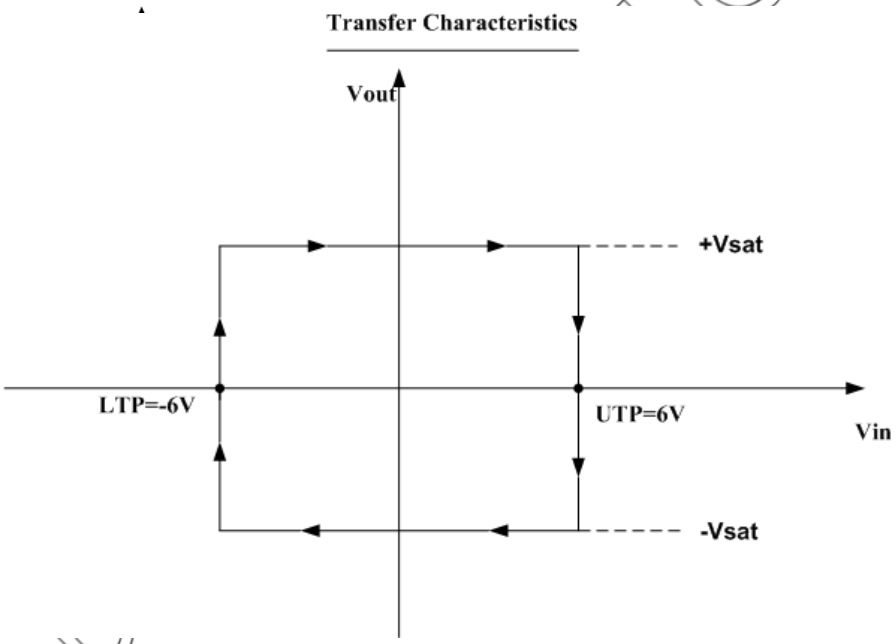
UTP = V_{sat} * $R_2/[R_1+R_2]$ and LTP = $(-V_{sat})$ * $R_2/[R_1+R_2]$

Let R_1 = 1 kΩ and V_{sat} = 12 V then, R_2 = 1 kΩ

CIRCUIT DIAGRAM:



EXPECTED WAVEFORMS AND HYSTERESIS CURVE:



Experiment No. 8

FULL-WAVE CONTROLLED RECTIFIER USIGNG RC TRIGGERING CIRUIT

AIM:

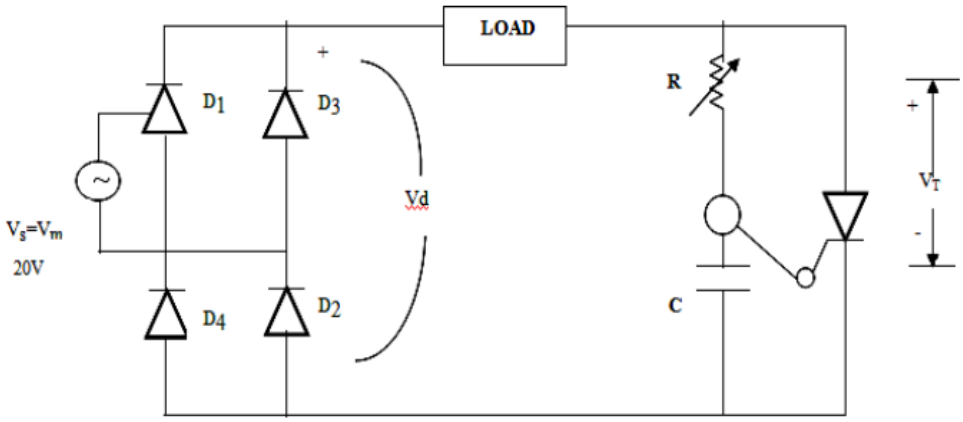
To design and test a full-wave controlled rectifier using RC triggering circuit.

APPARATUS REQUIRED:

RC firing circuit module, CRO, patch chords.

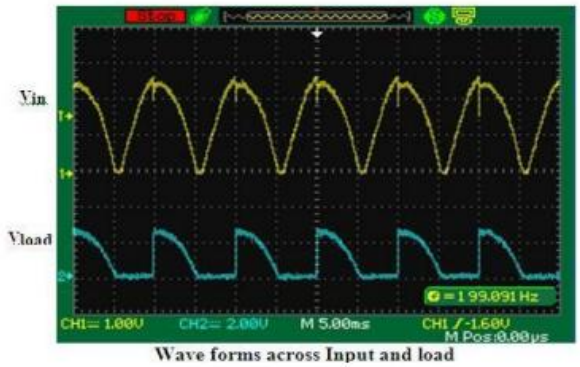
PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Connect a rheostat of 100 Ω between the load points.
3. Vary the control pot and observe the voltage waveforms across the load and SCR at different points of the circuit and also note down the SCR firing angle.
4. Draw the waveforms across the load and Thyristor for different firing angle.

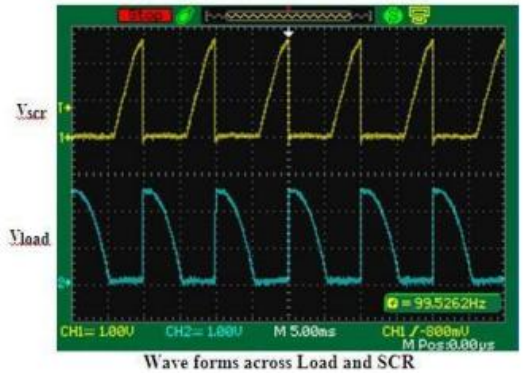


TABULAR COLUMN:

Time (in sec)	Firing angle	Load voltage	SCR voltage



Wave forms across Input and load



Wave forms across Load and SCR

RESULT:

Experiment No. 9

PRECISION HALF-WAVE AND FULL-WAVE RECTIFIERS USING OP-AMPS

AIM:

To design and test the precision half wave and full wave rectifiers using op-amps.

(A) Precision Half Wave Rectifier:

DESIGN:

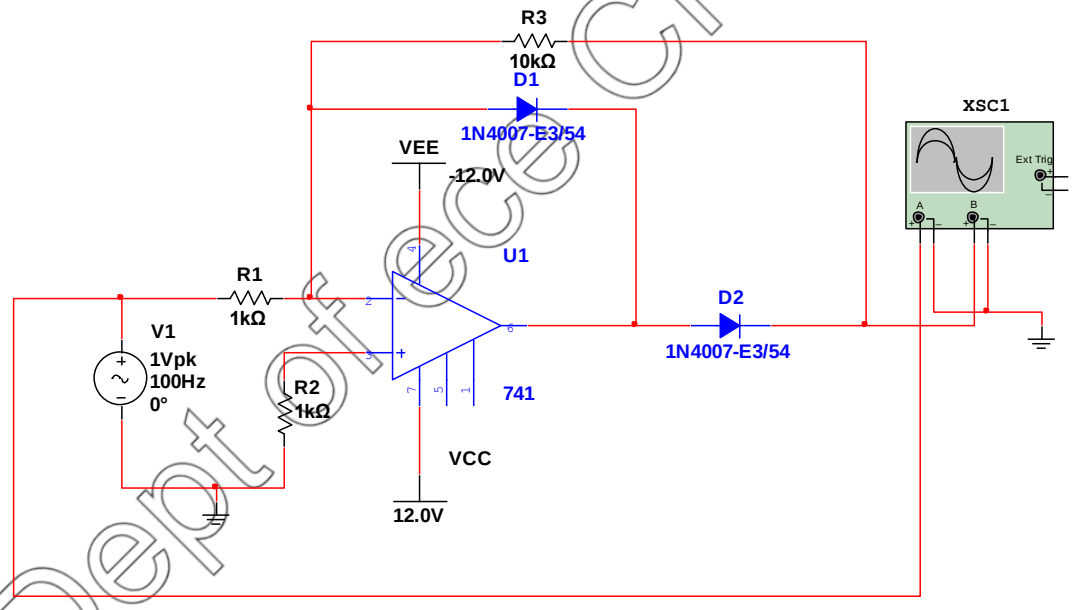
Choose $R_F=10R_1$, gain = $R_F/R_1=10$

If Vi =$0.5V_{p-p}$ then Vo =–5Vp-p Let $R_1=1K$, then $R_F=10$ K

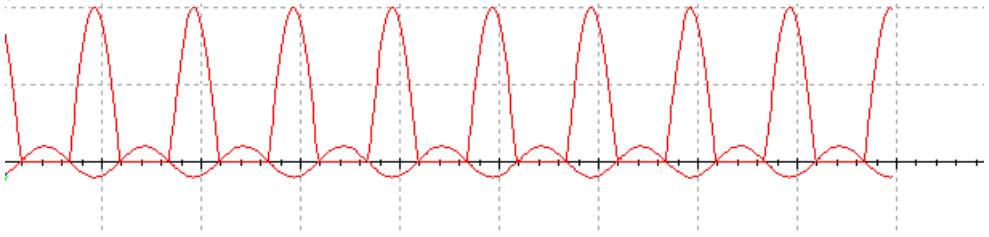
PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Observe the output waveform and measure the output frequency.

CIRCUIT DIAGRAM:



EXPECTED GRAPH:



(B) Precision Full Wave Rectifier:

DESIGN:

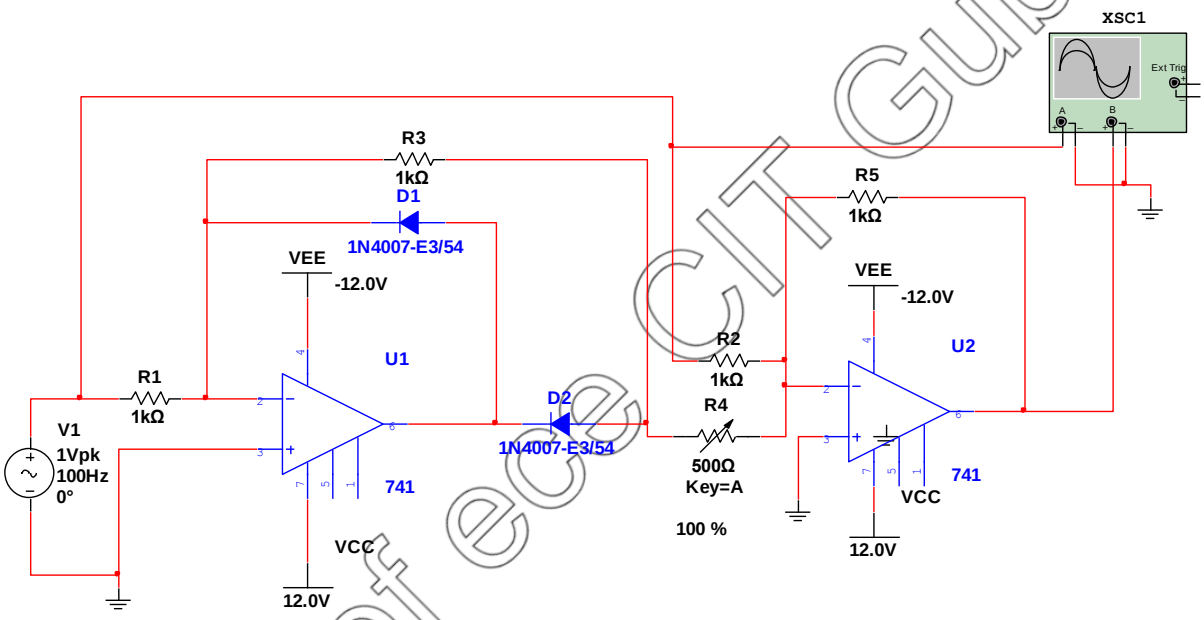
ChooseR_1 =R_2=R_3 =R_4=R=1KΩ R_5=R/2=500Ω.

ChooseR_5 =470Ω

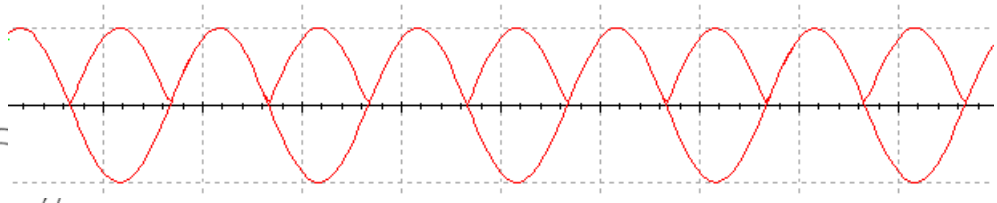
PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Observe the output waveform and measure the output frequency.

CIRCUIT DIAGRAM:



EXPECTED GRAPH:



RESULT:

Experiment No. 10

RC PHASE SHIFT OSCILLATOR

AIM:

To design and test the RC phase shift oscillator and determine the frequency of oscillation.

DESIGN:

$R_1=R_2=R_3=R_6=12k and A_{CL}=29 Find$

$R_4=A_{CL}*R1$

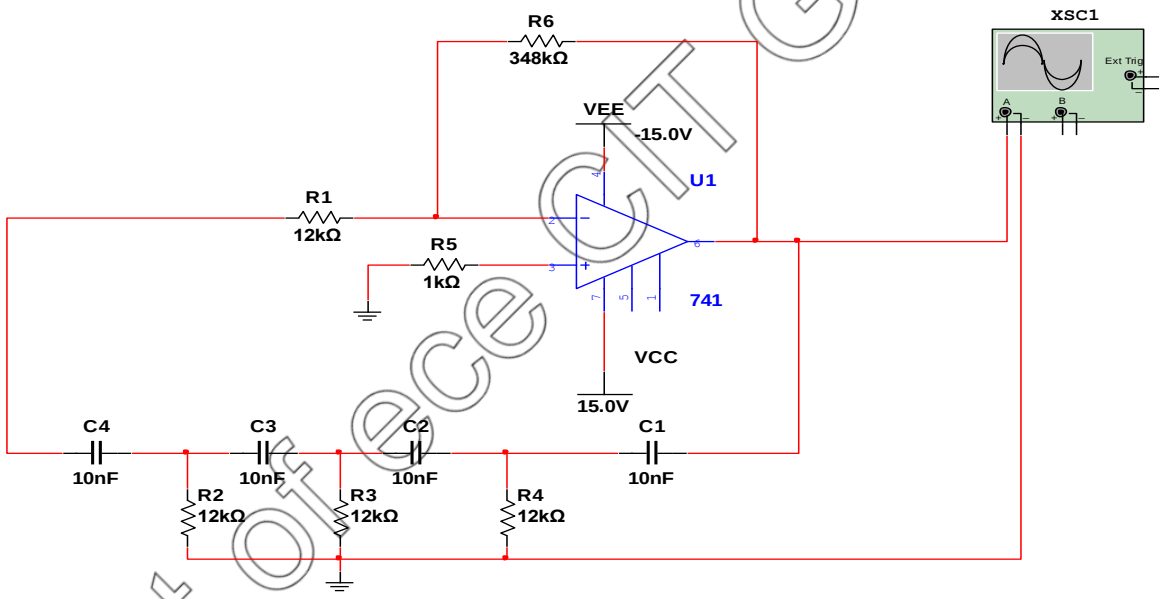
$R_5=1k, f=500Hz$

$f=1/2\pi RC\sqrt{6} Calculate$

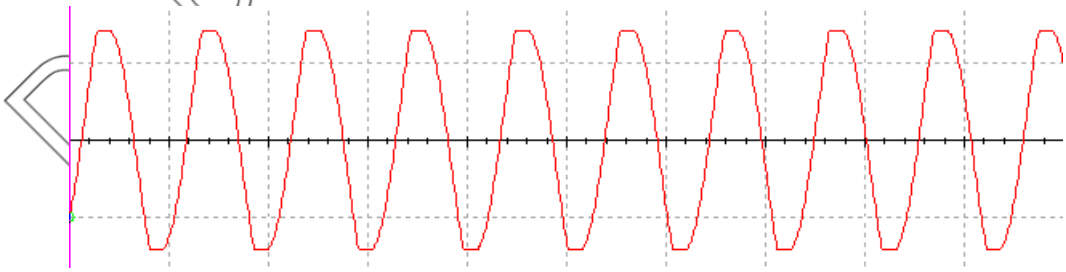
$C=1/2\pi Rf\sqrt{6}$

PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Observe the output waveform and measure the output frequency.



EXPECTED GRAPH:



RESULT: