Channabasaveshwara Institute of Technolog
(Affiliated to VTU, Belgaum & Approved by AICTE, New Delhi)
(NAAC Accredited & ISO 9001:2015 Certified Institution)
NH 206 (B.H. Road), Gubbi, Tumkur – 572 216. Karnataka

Department of Electronics & Communication Engineering

ANALOG AND DIGITAL SYSTEMS DESIGN LABORATORY

BECL305

B.E - III Semester Lab Manual

2024-25

Name : _____

USN : _____

Batch :_____Section : _____

Channabasaveshwara Institute of Technology
(Affiliated to VTU, Belgaum & Approved by AICTE, New Delhi)
(**NAAC Accredited & ISO 9001:2015 Certified Institution)**
NH 206 (B.H. Road), Gubbi, Tumkur – 572 216. Karnataka

Department of Electronics & Communication Engineering

Analog and Digital Systems Design Laboratory

Version 2.0

August 2024

Prepared by:

1. Mr. Maltesh Bajantri
   Asst. Prof., Dept. of ECE
2. Mrs. Bhavya B
   Asst. Prof., Dept. of ECE

Reviewed by:

Mr. Harsha G
Asst. Prof ., Dept. of ECE

Approved by:

Dr. Thejaswini R

Professor & Head, Dept. of ECE

INSTITUTE VISION

To create centres of excellence in education and to serve the society by enhancing the quality of life through value based professional leadership.

INSTITUTE MISSION

- To provide high quality technical and professionally relevant education in a diverse learning environment.
- To provide the values that prepare students to lead their lives with personal integrity, professional ethics and civic responsibility in a global society.
- To prepare the next generation of skilled professionals to successfully compete in the diverse global market.
- To promote a campus environment that welcomes and honors women and men of all races, creeds and cultures, values and intellectual curiosity, pursuit of knowledge and academic integrity and freedom.
- To offer a wide variety of off-campus education and training programmes to individuals and groups.
- To stimulate collaborative efforts with industry, universities, government and professional societies.
- To facilitate public understanding of technical issues and achieve excellence in the operations of the institute.

QUALITY POLICY

Our organization delights customers (students, parents and society) by providing value added quality education to meet the national and international requirements. We also provide necessary steps to train the students for placement and continue to improve our methods of education to the students through effective quality management system, quality policy and quality objectives.

Channabasaveshwara Institute of Technology

(Affiliated to VTU, Belgaum & Approved by AICTE, New Delhi)

(NAAC Accredited & ISO 9001:2015 Certified Institution)

NH 206 (B.H. Road), Gubbi, Tumkur – 572 216. Karnataka

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Vision

To create globally competent Electronics and Communication Engineering professionals with ethical and moral values for the betterment of the society

Mission

- To nurture the technical/professional/engineering and entrepreneurial skills for overall self and societal upliftment through co-curricular and extra-curricular events.
- To orient the Faculty/Student community towards the higher education, research and development activities.
- To create the Centres of Excellence in the field of electronics and communication in collaboration with industries/Universities by training the faculty through latest technologies.
- To impart quality technical education in the field of electronics and communication engineering to meet over the current/future global industry requirements.

Program Objectives (PO's)

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Educational Objectives (PEO's)

After four Years of Graduation, our graduates are able to:

- Provide technical solutions to real world problems in the areas of electronics and communication by developing suitable systems.
- Pursue engineering career in Industry and/or pursue higher education and research.
- Acquire and follow best professional and ethical practices in Industry and Society.
- Communicate effectively and have the ability to work in team and to lead the team.

Program Specific Outcomes (PSO's)

At the time of graduation, our graduates are able to:

- **PSO1**: Build Analog and Digital Electronic systems for Multimedia Applications, VLSI and Embedded Systems in Interdisciplinary Research / Development.
- **PSO2**: Design and Develop Communication Systems as per Real Time Applications and Current Trends.

Channabasaveshwara Institute of Technology

(Affiliated to VTU, Belgaum & Approved by AICTE, New Delhi)
(NAAC Accredited & ISO9001:2015 Certified Institution)
NH 206 (B.H.Road), Gubbi, Tumkur – 572 216. Karnataka.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SYLLABUS

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)
SEMESTER – III

ANALOG AND DIGITAL SYSTEMS DESIGN LABORATORY			
Laboratory Code	BECL305	**CIE Marks**	**50**
Number of Lecture Hours/Week	0:0:2:0	**SEE Marks**	**50**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 01

Laboratory Experiments

1. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
2. Design and set-up BJT/FET
   a. i) Colpitts Oscillator, ii) Crystal Oscillator
3. Design and set up the circuits using op amp:
   a. i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator
4. Design 4-bit R – 2R Op-Amp Digital to Analog Converter for (i) a 4-bit binary input using toggle switches (ii) by generating digital inputs using mod16.
5. Design and implement
   a. Half Adder & Full Adder using basic gates and NAND gates,
   b. Half subtractor & Full subtractor using NAND gates,
      i. (c) 4-variable function using IC74151 (8:1MUX).
6. Realize
   a. Binary to Gray code conversion & vice-versa (IC74139),
   b. (ii) BCD to Excess-3 code conversion and vice versa
7. Realize using NAND Gates:
   a. Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop

i. Realize the shift registers using IC7474/7495:

b. (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.

8. Realize
   i. Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop
   ii. Mod-N Counter using IC7490 / 7476
   iii. Synchronous counter using IC74192

Demonstration Experiments

9. Design and test the following using 555 timer
   i) Monostable Multivibrator
   ii) Astable Multivibrator

10. Design and Test the second order Active Filters and plot the frequency response,
    i) Low pass Filter
    ii) High pass Filter

11. Design and Test a Regulated Power supply

12. Design and test an audio amplifier by connecting a microphone input and observe the output using a loudspeaker.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Channabasaveshwara Institute of Technology

(Affiliated to VTU, Belgaum & Approved by AICTE, New Delhi)
(NAAC Accredited & ISO9001:2015 Certified Institution)
NH 206 (B.H.Road), Gubbi, Tumkur – 572 216. Karnataka.

Department of Electronics and Communication Engineering

ANALOG AND DIGITAL ELECTRONICS LABORATORY: Course Objectives and Outcomes

---

COURSE OBJECTIVES:

The main objectives of this lab are,

1. Understand the electronic circuit schematic and its working
2. Realize and test amplifier and oscillator circuits for the given specifications
3. Realize the op amp circuits for the applications such as DAC, implement mathematical Functions and precision rectifiers.
4. Design and test the combinational and sequential logic circuits for their functionalities.
5. Use the suitable ICs based on the specifications and functions.

COURSE OUTCOMES:

After completing this course the student could be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Opamp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic circuit experiments using 555 timer.

‘Instructions to the Candidates’

- Student should come with thorough preparation for the experiment to be conducted.
- Student should take prior permission from the concerned faculty before availing the leave.
- Student should come with proper dress code and to be present on time in the laboratory.
- Student will not be permitted to attend the laboratory unless they bring the practical record fully completed in all respects pertaining to the experiment conducted in the previous class.
- Student will not be permitted to attend the laboratory unless they bring the observation book fully completed in all respects pertaining to the experiment to be conducted in present class.
- Experiment should be started conducting only after the staff-in-charge has checked the circuit diagram.
- All the calculations should be made in the observation book. Specimen calculations for one set of readings have to be shown in the practical record.
- Wherever graphs to be drawn, A-4 size graphs only should be used and the same should be firmly attached in the practical record.
- Practical record and observation book should be neatly maintained.
- Student should obtain the signature of the staff-in-charge in the observation book after completing each experiment.
- Theory related to each experiment should be written in the practical record before procedure in your own words with appropriate references.

CONTENTS

INDEX PAGE

Sl. No	Name of the Experiment	Date			Manual Marks	Record Marks (Max. 10)	Signature (Student)	Signature (Faculty)
		Conduction	Repetition	Submission of Record				
1	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.							
2	Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator							
3	Design and set up the circuits using opamp: b. i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator							
4	Obtain the static characteristics of SCR and test SCR Controlled HWR and FWR using RC Triggering circuit.							
5	Design and implement Half Adder & Full Adder using basic gates and NAND gates, Half subtractor & Full subtractor using NAND gates, 4-variable function using IC74151(8:1MUX).							
6	Realize							

	Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion and vice versa							
7	Realize using NAND Gates: Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-FlopRealize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.							
8	Realize Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop Mod-N Counter using IC7490 / 7476 Synchronous counter using IC74192							
9	Design 4-bit R – 2R Op-Amp Digital to Analog Converter for a 4-bit binary input using toggle switches							
10	Pseudorandom sequence generator using IC7495							
11	Test the precision rectifiers using opamp: i) Half wave rectifier ii) Full wave rectifier							
12	Design and test Monostable and Astable Multivibrator using 555 Timer							
Average								

Experiment No. 1 **Date:**

COMMON-EMITTER AMPLIFIER

AIM:

To design and set up the common emitter amplifier under voltage divider bias with and without feedback and determine the input/output impedance and gain bandwidth product from its frequency response.

COMPONENTS REQUIRED:

Transistor SL 100, Resistors, Capacitor, Power supply, CRO, etc.

DESIGN:

If Q point is not given (# Q2), then assume a suitable value, say: (Vce, Ic) = (5V, 5mA).
For SL-100, β =100. Let Vcc = 10V

R_E:
V_{RE} = Vcc /10 =10V/10 = 1V
i.e. $I_E R_E$ =1V
$R_E = 1/I_E = 1/I_C$ Since $I_E = I_C$
Therefore, R_E = 1/5mA = 200Ω. Choose (R_E =220Ω) as standard value

R_C:
Applying KVL in CE loop, we have,
$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$
$I_C R_C = V_{CC} - V_{CE} - V_{RE} = 10 - 5 - 1$, $I_C R_C$ = 4V
Therefore Rc = 4 / I_C = 4 /5mA = 800Ω . Choose Rc = 820Ω as std value

R_1:
From the above biasing circuit we have
$V_B = V_{BE} + V_{RE}$ = 0.7 + 1 = 1.7V (V_{BE} = 0.7V for Si)
We have $I_C = \beta I_B$ So, I_B = 50μA

Assume 10I_B flows through R_1
Therefore R_1 =Vcc – V_B / 10 I_B = (10 –1.7) / (10 × 50μA) = 16.6KΩ.
Choose R_1 = 18 KΩ as Std value

R_2:

$R_2 = V_B / 9I_B = 1.7 / (9 \times 50\mu A) = 3.77\ K\Omega$ choose $R_2 = 4.7\ K\Omega$ as standard value

CE: [Bypass capacitor]

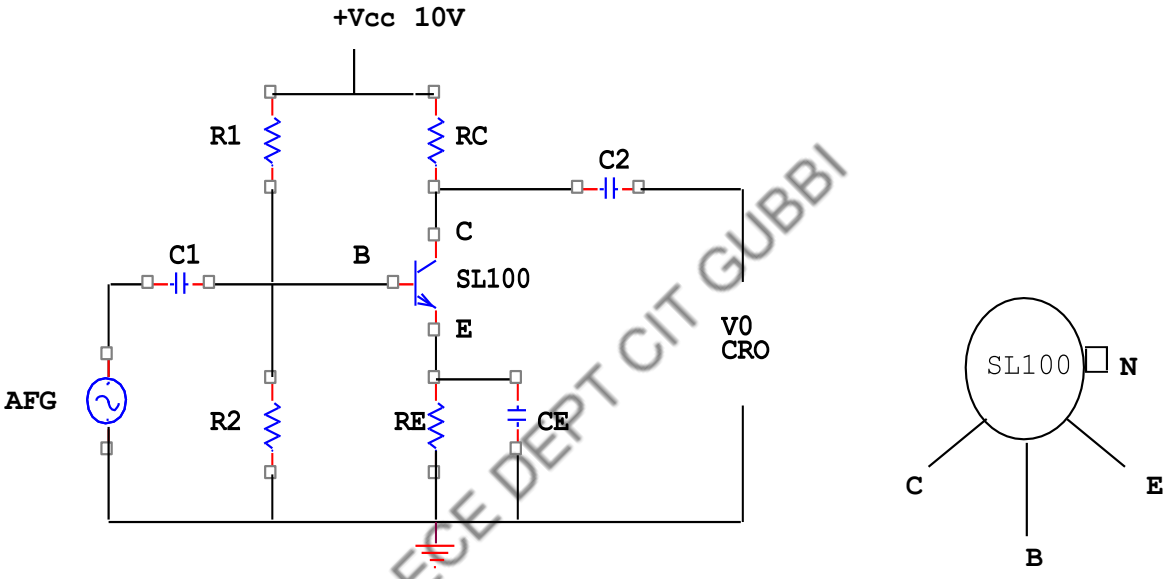
Let $X_{CE} = R_E / 10$; $1 / 2\pi f C_E = R_E / 10$ therefore $C_E = 10 / 2\pi f R_E$

At f = 100KHz, we have $C_E = 10 / 2 \times 3.14 \times 100 \times 220 = 72.34\ \mu F$

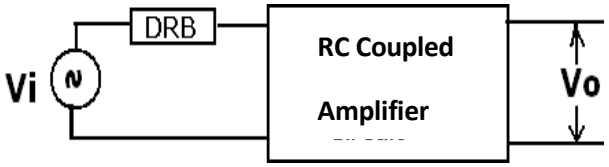
Choose $C_E = 100\mu F$ as Std value

Choose C1 = C2 = 0.1 µF => coupling capacitors

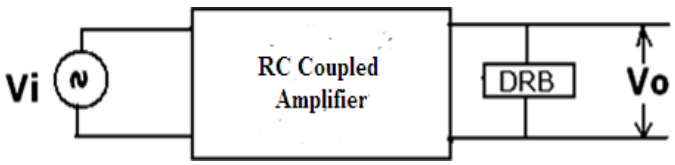
CIRCUIT DIAGRAM:



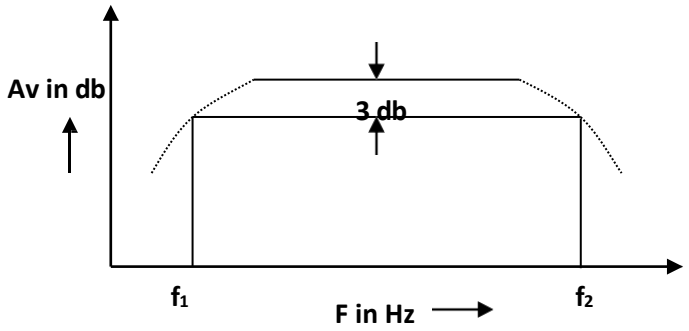
To measure Z_i :



To measure Z_0 :



Frequency Response:



f_1 →Lower cut off frequency

f_2 →Upper cutoff frequency

Av →Voltage gain

Av →Voltage gain at mid band

f_2–f_1 → Bandwidth of the amplifier

TABULAR COLUMN:

Input voltage Vin (p-p) = ……

Frequency (Hz)	Out put (p-p) V	Voltage gain (V_O/Vi)	Gain=20 log(Vo/Vi)

PROCEDURE:

1. Make the connections as shown in the figure.
2. To find Q point set V_{CC} = 10V and without applying the input signal (Vin = 0V) measure the DC voltage using CRO at the collector V_C and emitter V_E with respect to ground.
3. Keep the input signal amplitude slightly less than maximum signal handling capacity. (Max signal handling Capacity is the input voltage at which output gets clipped).
4. Vary the frequency and note down the output up to 1 MHz.
4. Plot the frequency response on semi log sheet.

CE amplifier with feedback

- Remove the bypass capacitor C_E. This is a negative feedback circuit.
- Repeat the above procedure.

To find frequency response:

1. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
2. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
3. Calculate A_V and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and bandwidth.
4. Calculate figure of merit.

To find the input impedance (Z_i) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10 kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance.

To find the output impedance (Zo) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10 kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.

RESULT:

Experiment No. 2 **Date:**

COLPITTS AND CRYSTAL OSCILLATORS

AIM:

To design and setup the following tuned oscillator circuits using BJT, and determine the frequency of oscillation. (a). Colpitts Oscillator (b) Crystal Oscillator

APPARATUS:

Resistors, Transistor SL100, 1KΩ Pot, Capacitor, Inductance Box, CRO, Power supply

(A). COLLPITT'S OSCILLATOR

DESIGN:

If Q point is not given (# Q2), then assume a suitable value say (Vce, Ic) = (5V, 5mA)
For SL-100, β =100 Let Vcc = 10V

R_E:
V_{RE} = Vcc /10 =10V/10 = 1V. i.e. $I_E R_E$ = 1V
$R_E = 1/I_E = 1/I_C$ Since $I_E = I_C$
Therefore, R_E = 1/5mA = 200Ω. Choose R_E =220Ω as standard value

R_C:
Applying KVL in CE loop, we have, $V_{CC} – I_C R_C – V_{CE} – V_{RE} = 0$
$I_C R_C = V_{CC} – V_{CE} – V_{RE}$ = 10 – 5 – 1, $I_C R_C$ = 4V
Therefore Rc = 4 / IC = 4 /5mA = 800Ω .Choose Rc = 820Ω as std value

R_1:
From the above biasing circuit we have $V_B = V_{BE} + V_{RE}$ = 0.7 + 1 = 1.7V (V_{BE} = 0.7V)
We have $I_C = \beta I_B$ So, I_B = 50μA
Assume $10I_B$ flows through R_1
Therefore R_1 =Vcc – V_B / 10 I_B = (10 –1.7) / (10 × 50μA) = 16.6KΩ.
Choose R_1 = 18 KΩ as Std value

R_2:
$R_2 = V_B / 9I_B$ = 1.7 / (9×50μA) = 3.77 KΩ choose R_2 = 4.7 KΩ as std value

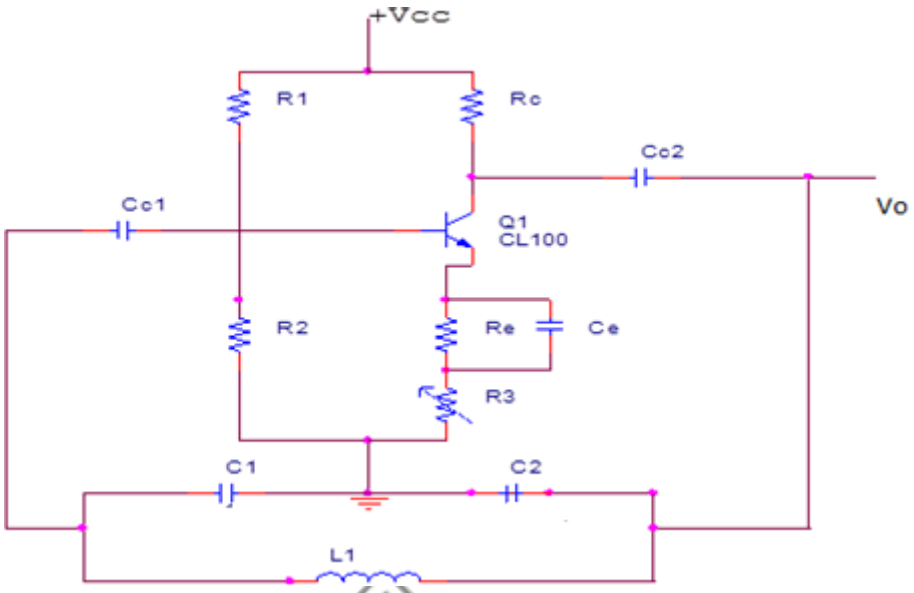
Let $X_{CE} = R_E /10$; $1 / 2\pi f C_E = R_E / 10$ therefore $C_E = 10 / 2\pi f R_E$
At f = 100KHz, we have C_E = 10 / 2 ×3.14 × 100 × 220 = 72.34 μF

Choose C_E = 100μF as Std value

Assume C_1 = 0.01μF, C_2 = 0.01μF, f = 100 KHz

$f = \frac{1}{2\pi\sqrt{LC}}$ where $C = \frac{C_1 C_2}{C_1 + C_2}$ L =500μH

CIRCUIT DIAGRAM:



PROCEDURE:

1. Make the connections as shown in the figures
2. Check the DC bias condition of amplifier
3. Set the value of inductor and capacitor for designed frequency after connecting the tank circuit.
4. Adjust CRO to get proper output.
5. Measure the amplitude and frequency of the signal.

RESULT:

Peak to peak voltage of Colpitt's oscillator =

Frequency as measured in Colpitt's oscillator =

(B). CRYSTAL OSCILLATOR

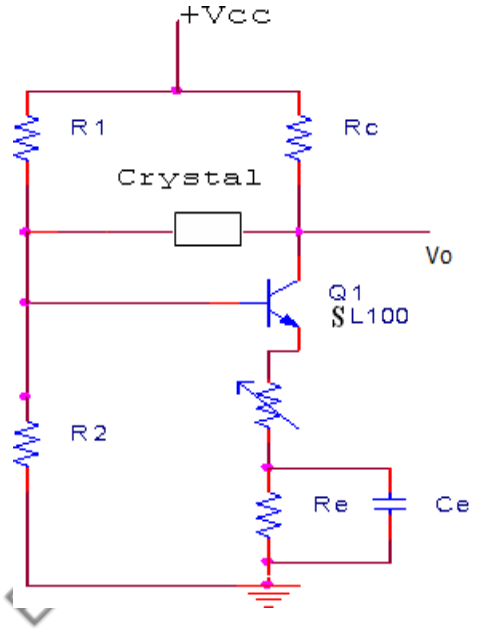
AIM:

To design and setup the crystal oscillator and determine the frequency of oscillation

APPARATUS:

Transistor SL 100, Resistors 27K, 4.7K, 1K, 270Ω, Capacitors 0.47μF, 47μF
Crystal, Power Supply, CRO

CIRCUIT DIAGRAM:



DESIGN:

If Q point is not given (# Q2), then assume a suitable value say (Vce, Ic) = (5V, 5mA)
For SL-100, β =100 Let Vcc = 10V

R_E:

V_{RE} = Vcc /10 =10V/10 = 1V. i.e. $I_E R_E$ = 1V
$R_E = 1/I_E = 1/I_C$ Since $I_E = I_C$
Therefore, R_E = 1/5mA = 200Ω. Choose R_E =220Ω as standard value

R_C:

Applying KVL in CE loop, we have, $V_{CC} – I_C R_C – V_{CE} – V_{RE} = 0$
$I_C R_C = V_{CC} – V_{CE} – V_{RE} = 10 – 5 – 1$, $I_C R_C$ = 4V

Therefore Rc = 4 / IC = 4 /5mA = 800Ω .Choose Rc = 820Ω as std value

R_1:
From the above biasing circuit we have $V_B = V_{BE} + V_{RE} = 0.7 + 1 = 1.7V$ ($V_{BE} = 0.7V$)
We have $I_C = \beta I_B$ So, $I_B = 50\mu A$
Assume $10I_B$ flows through R_1
Therefore $R_1 = Vcc - V_B / 10 I_B = (10 - 1.7) / (10 \times 50\mu A) = 16.6K\Omega$.
Choose R_1 = 18 KΩ as Std value

R_2:
$R_2 = V_B / QI_B = 1.7 / (9 \times 50\mu A) = 3.77$ KΩ choose R_2 = 4.7 KΩ as std value
Let $X_{CE} = R_E /10$; $1 / 2\pi fC_E = R_E / 10$ therefore $C_E = 10 / 2\pi fR_E$
At f = 100KHz, we have $C_E = 10 / 2 \times 3.14 \times 100 \times 220 = 72.34$ μF
Choose C_E = 100μF as Std value
Choose C1 = C2 = 0.1 μF => coupling capacitors

PROCEDURE:
1. Rig up the circuit as shown in the circuit diagram.
2. Adjust CRO to obtain proper sinusoidal output waveform.
3. Measure frequency of oscillations and compare with designed value.

RESULT:

Theoretical frequency =
Practical frequency =
Amplitude =

Experiment No. 3(a) **Date:**

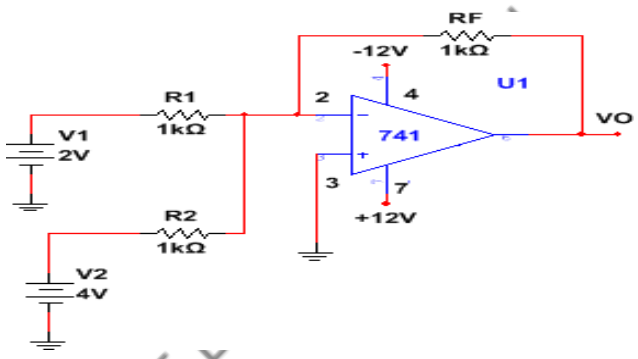
SUMMING AMPLIFIER

AIM: To design Summing Amplifier (Adder) using Op-Amp

APPARATUS:

Name	Description	Qty
Op Amp	µA741	1
Resistors	1 KΩ	3
DC Power Supply	-	3

CIRCUIT DIAGRAM:



DESIGN:

$V_0 = -(V_1/R_1 + V_2/R_2)$

Let $R_1 = R_2 = R_F = 1\text{k}\Omega$

PROCEDURE:

1. Rig up the circuit as shown in figure.
2. Apply input V_1=0.5V and V_2=0.5V
3. Measure the output using multimeter and compare it with theoretical value.
4. Apply different values of V_1 and V_2 and note down the output.

RESULT:

Sl No	Input V_1 (V)	Input V_2 (V)	Theoretical output(V)	Practical output(V)
1				
2				

Experiment No. 3 (b)

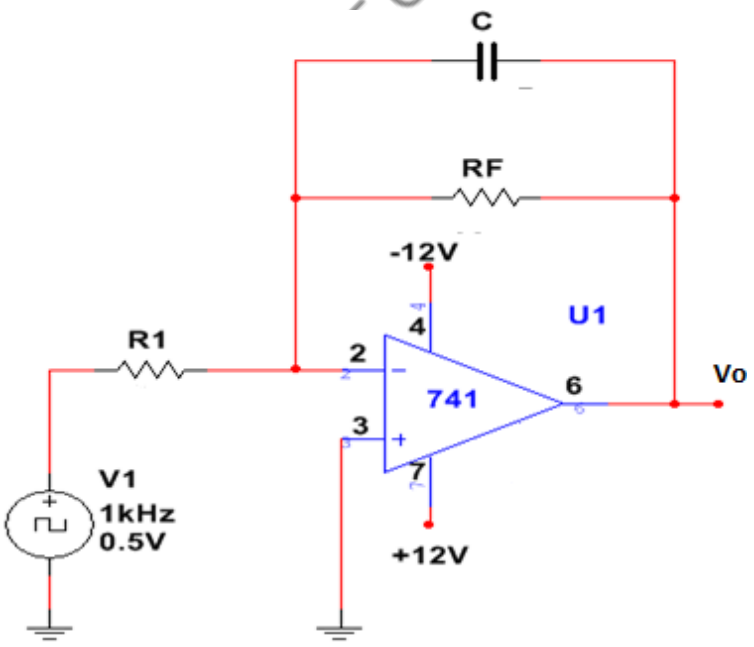
INTEGRATOR

AIM: To design Integrator using Op-Amp

APPARATUS:

Name	Description	Qty
Op Amp	µA741	1
Resistors	100 KΩ 10 KΩ	1 1
Capacitor	0.01 µF	1
AFO	-	1
CRO	-	1
DC Power Supply	-	1

CIRCUIT DIAGRAM:



DESIGN:

$V_0 = 1/R_1 \int_0^T V_{in}\, dt$

For an Integrator, $R_1C \gg T$, $R_1C = 10T$

Assume C= 0.01µF and T= 1ms then compute R1

Gain limiting can be produced by shunting the integrator capacitor with a resistor

This resistor sets the upper limit voltage gain to $A_{max} = -\frac{R_F}{R1}$

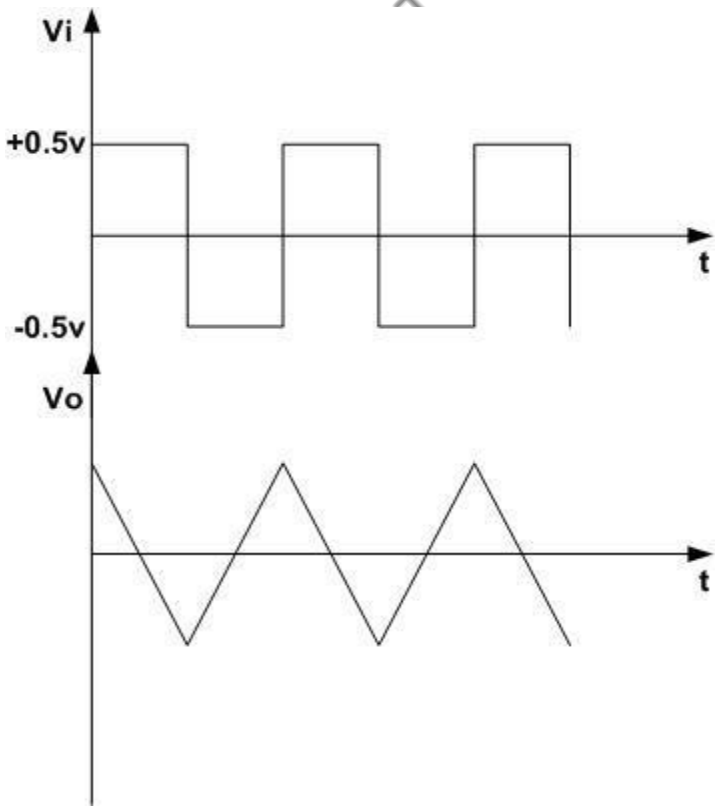
Choose R_F= 10 R1 then R_F= 100 kΩ

Critical frequency is that frequency above which the circuit act like an integrator and it is given by $f_{low} = \frac{1}{2\pi R_F C}$.

PROCEDURE:

1. Rig up the circuit as shown in figure.
2. Apply the input Square wave of 0.5 V, 1KHz
3. Observe the output on CRO

EXPECTED WAVEFORMS:



Experiment No. 3 (c)

DIFFERENTIATOR

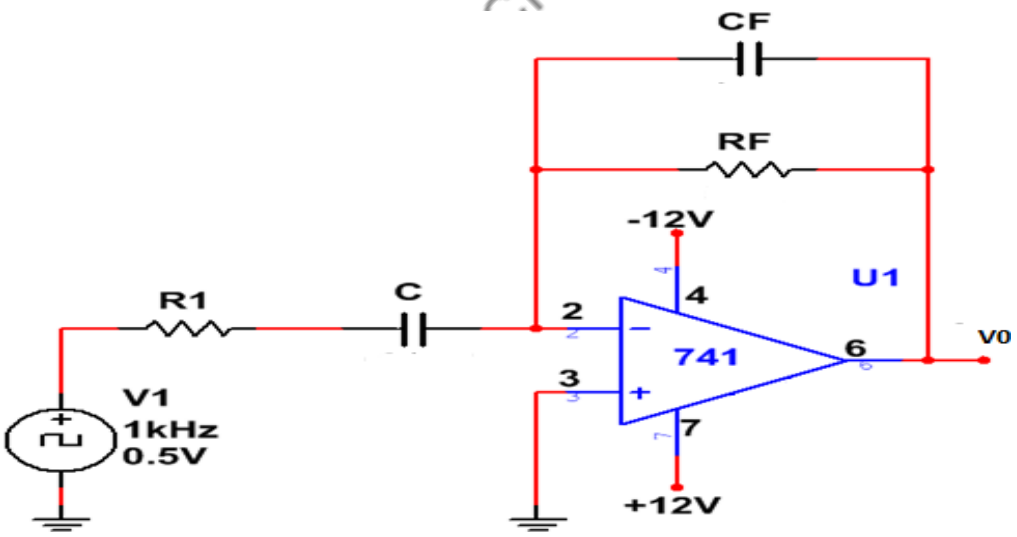
AIM:

To design Differentiator using Op-Amp

APPARATUS:

Name	Description	Qty
Op Amp	µA741	1
Resistors	100 Ω 5 KΩ	1 1
Capacitor	0.01 µF 1nF	1 1
AFO	-	1
CRO	-	1
DC Power Supply	-	1

CIRCUIT DIAGRAM:



DESIGN:

$V_0 = -R_f C \frac{dV}{dt}$

For an Differentiator, $R_f C \ll T$, $R_f C = \frac{T}{10}$

Assume C= 0.01µF and T= 1ms, compute R_f

Assume gain A=50, compute R_1

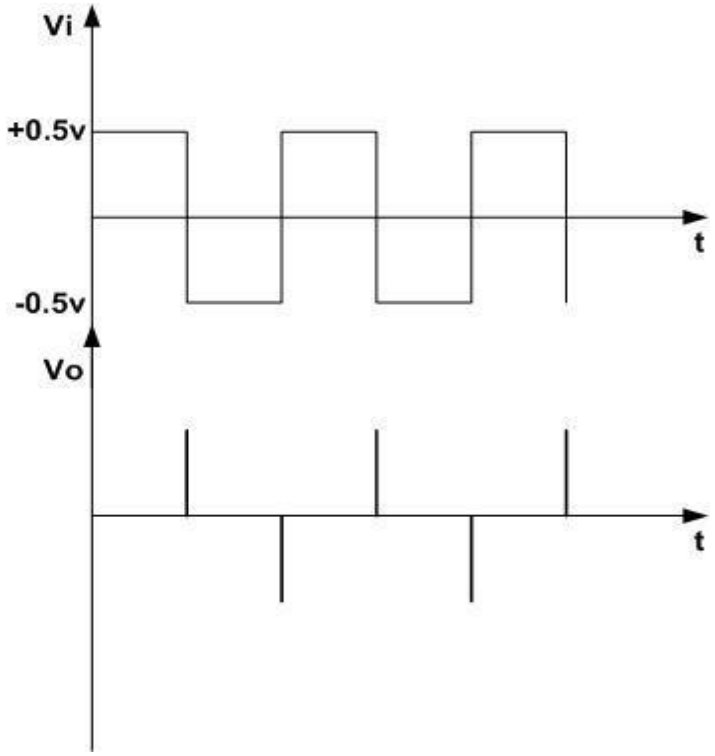
$F_{HIGH} = \frac{1}{2\pi R_f Cf}$. Where F_{HIGH} is the highest frequency for differentiator .

Hence choose C_f= 1nF

PROCEDURE:

1. Rig up the circuit as shown in figure.
2. Apply the input Square wave of 0.5 V, 1KHz
3. Observe the output on CRO

EXPECTED WAVEFORMS:



Experiment No. 3 (d)

COMPARATOR

AIM:

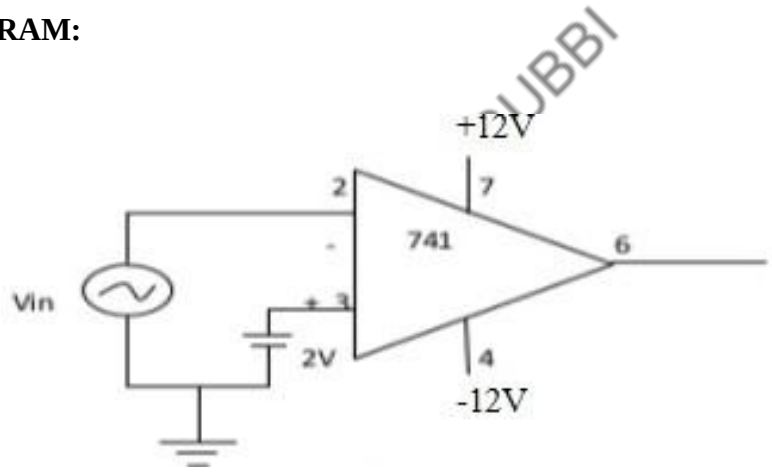
To test Comparator using Op-amp

APPARATUS:

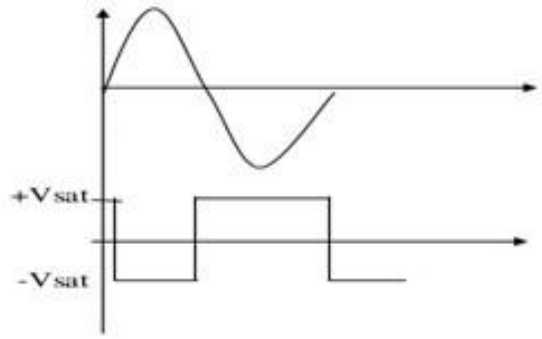
Name	Description	Qty
Op Amp	µA741	1
AFO	-	1
CRO	-	1
DC Power Supply	-	2

a) Comparator

CIRCUIT DIAGRAM:



EXPECTED WAVEFORMS



PROCEDURE:

1. Connect the circuit as shown in the figure
2. Apply the supply voltages of +15V to pin 7 and -15V to pin 4 of IC 741 respectively.
3. Set the reference voltage as 2V DC.
4. Apply sine wave of 10Vp-p with1KHz frequency from the function generator as Vi.
5. Check the output in CRO and calculate the amplitude of the output wave form.
6. Compare the output wave form amplitude with input signal amplitude.

RESULT:

Experiment No. 4

R-2R DAC USING OP-AMP

AIM: To Design 4 bit R-2R Op-Amp DAC using 4 bit binary input from toggle switches

Apparatus Required:

Sl. No.	Particulars	Specification	Quantity
1.	IC	µA741	01
2.	Resistors	As per design	-
3.	Multimeter	-	01
4.	Base board + connecting wires	-	01 Set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-6.
3. Digital input data is given at D3, D2, D1, D0 and corresponding analog output voltage V_0 is measured using voltmeter.
4. Tabulate the readings & plot the graph of V_{in} v/s V_o.

Note:

1. Do.D1.D2 & D3 are binary input.
2. V_o is the analog output.
3. Binary input Di (i = 0 to 3) can be made '0' by connecting the i/p to ground. It can be made '1' by connecting to –5 V.

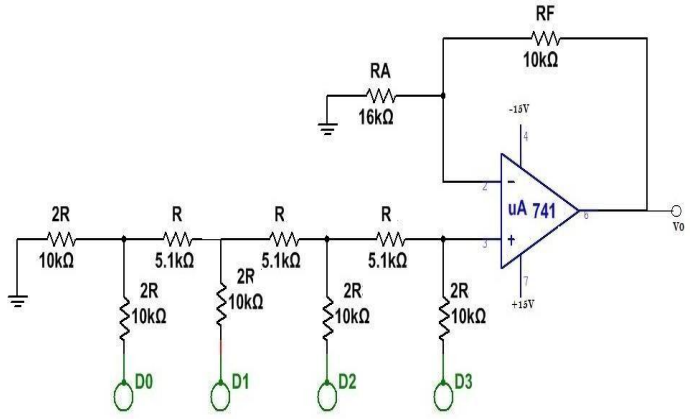
Logic 0- 0V

Logic 1 - +5V

Observation:

Decimal Value	Binary Inputs				Analog O/P Vo(volts) Theoretical values	Analog O/P Vo(volts) Practical values
	D_3	D_2	D_1	D_0		
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Circuit diagram:



Design Specification:

Design 4 bit R-2R DAC for an output voltage, V_0 = 5V, when the input is

$(10)_d$ [i.e., $(1010)_b$].

$D_3\ D_2\ D_1\ D_0$

$(10)_{10} = (1\ \ 0\ \ 1\ \ 0)_2$

Therefore $D_3 = 1$ (MSB), $D_2 = 0$, $D_1 = 1$, $D_0 = 0$ (LSB)

$$Av = \frac{Vo}{Vi} => Vo = Av.Vi$$

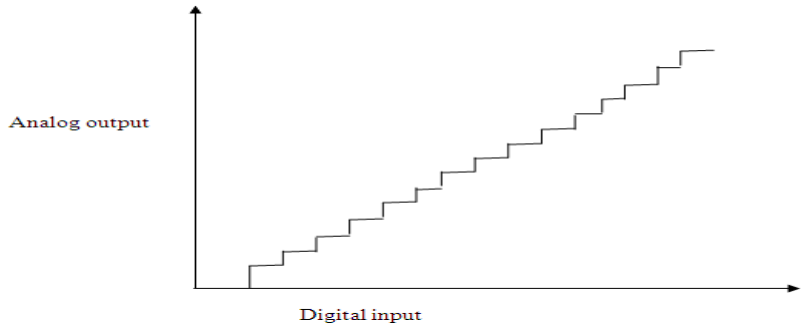
$$Vo = \left(1 + \frac{R_F}{RA}\right)\frac{Vref}{16}(D0 + 2D1 + 4D2 + 8D3)$$

Assume RF=10kΩ, Vref=5V

$$5 = \left(1 + \frac{10k}{RA}\right)\frac{5}{16}(2 * 1 + 8 * 1)$$

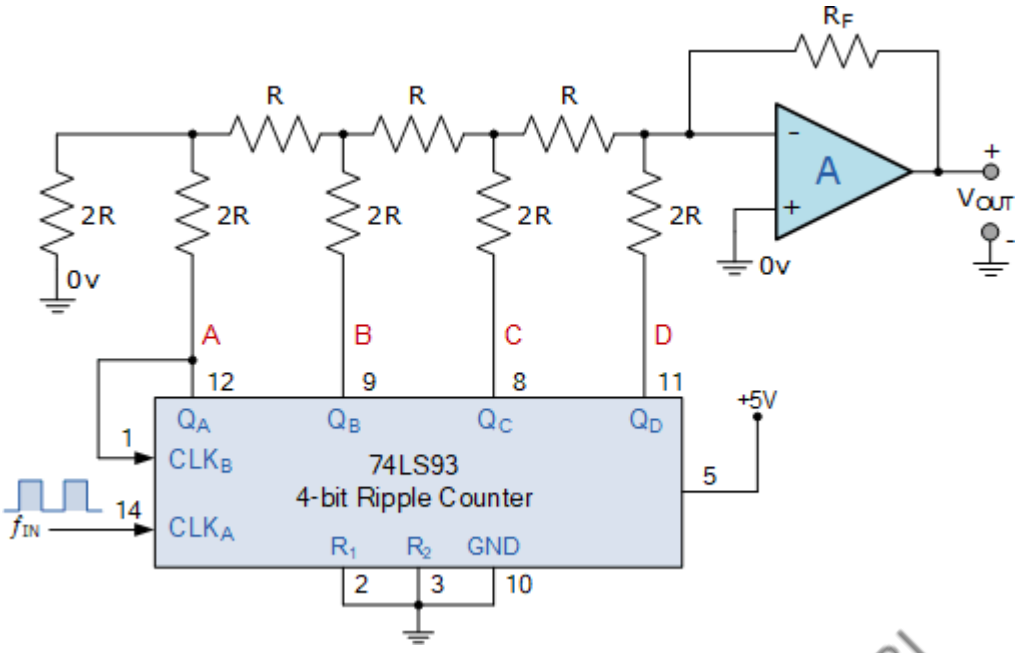
RA=16kΩ

EXPECTED WAVEFORM:



RESULT:

b) To Design 4 bit R-2R Op-Amp DAC by generating digital inputs using mod16



R=5kohm

Observation:

INPUT	Binary Inputs				Analog O/P Vo(volts) Theoretical values	Analog O/P Vo(volts) Practical values
	D_3	D_2	D_1	D_0		
CLK	0	0	0	0		
CLK	0	0	0	1		
CLK	0	0	1	0		
CLK	0	0	1	1		
CLK	0	1	0	0		
CLK	0	1	0	1		
CLK	0	1	1	0		
CLK	0	1	1	1		
CLK	1	0	0	0		
CLK	1	0	0	1		
CLK	1	0	1	0		
CLK	1	0	1	1		
CLK	1	1	0	0		
CLK	1	1	0	1		
CLK	1	1	1	0		
CLK	1	1	1	1		

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram.
3. The clock pulse is applies to the 4-bit ripple counter the digital outputs are generated in terms of D3, D2, D1, D0 Corresponding analog output voltage V_0 is measured using voltmeter.
4. Tabulate the readings & plot the graph of $_{Vin}$ v/s $_{Vo}$.

Experiment No: 5 **Date:**

ADDERS AND SUBTRACTORS

Aim: (i) To realize half/full adder using Logic gates & NAND gates

(ii) To realize half/full Subtractor using Logic gates & NAND gates

Components Required: IC 7408, IC 7432, IC 7486, IC 7404, IC 7400,

Patch cords

Theory:

Half-Adder: A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit S, and the other is the carry bit, C. The Boolean functions describing the half-adder are: $\mathbf{S = A \oplus B}$

$$\mathbf{C = A.B}$$

Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, C_{in} , is called a full-adder. The Boolean functions describing the full-adder are:

$$\mathbf{S = A \oplus B \oplus C_{in}}$$

$$\mathbf{C = A.B + C_{in}\ (A \oplus B)}$$

Half Subtractor: Subtracting a single-bit binary value B from another A (i.e. A-B) produces a difference bit D and a borrow out bit Br. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the half-Subtractor are:

$$\mathbf{D = A \oplus B}$$

$$\mathbf{B_r = A'.B}$$

Full Subtractor: Subtracting two single-bit binary values, B, Cin from asingle-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction. The Boolean functions describing the full- subtractor are:

$$\mathbf{D = A \oplus B \oplus C_{in}}$$

$$B_r = A'.B + A'.C_{in} + B.C_{in}$$

Half Adder

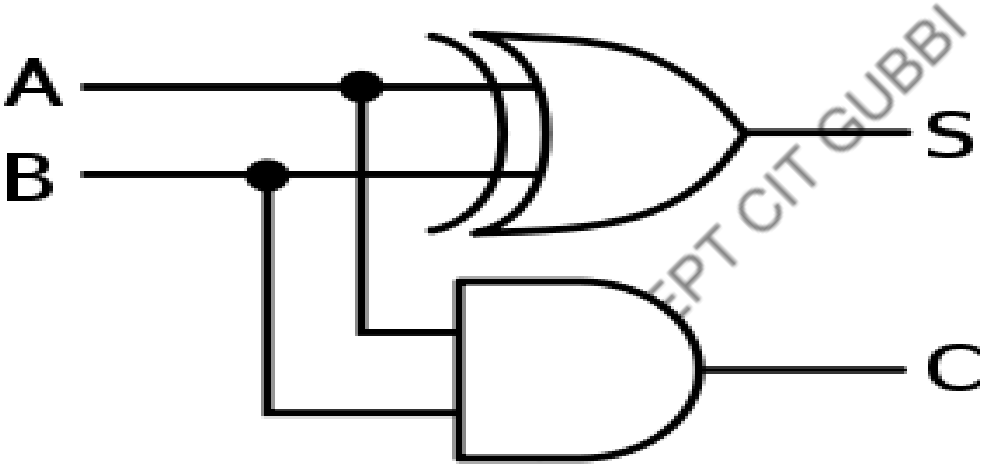
Truth Table:

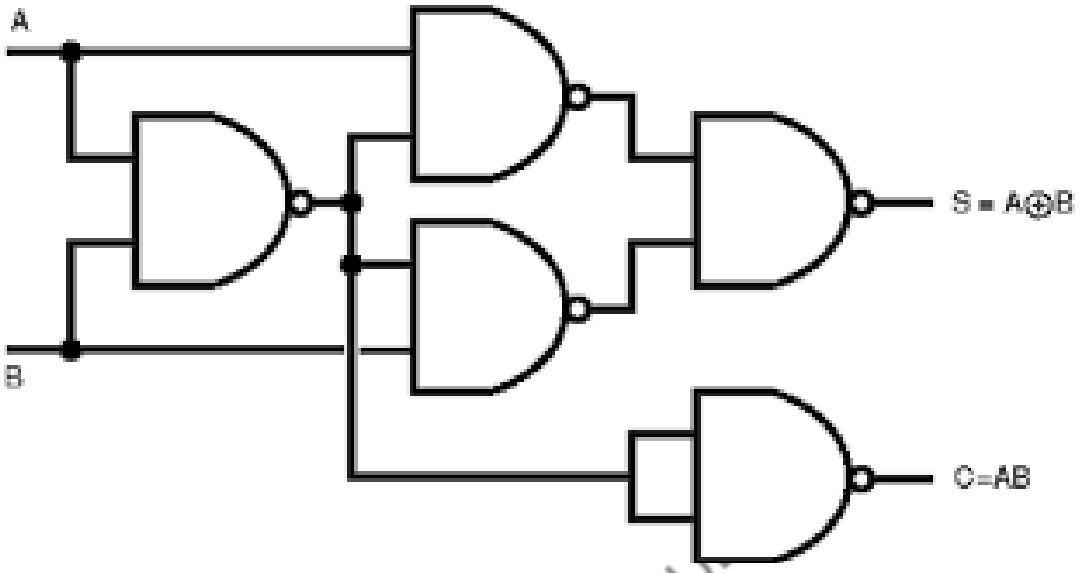
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

S =A $\oplus$ B

C = A.B

Realization of Half Adder:





Using NAND gates

1. Full Adder

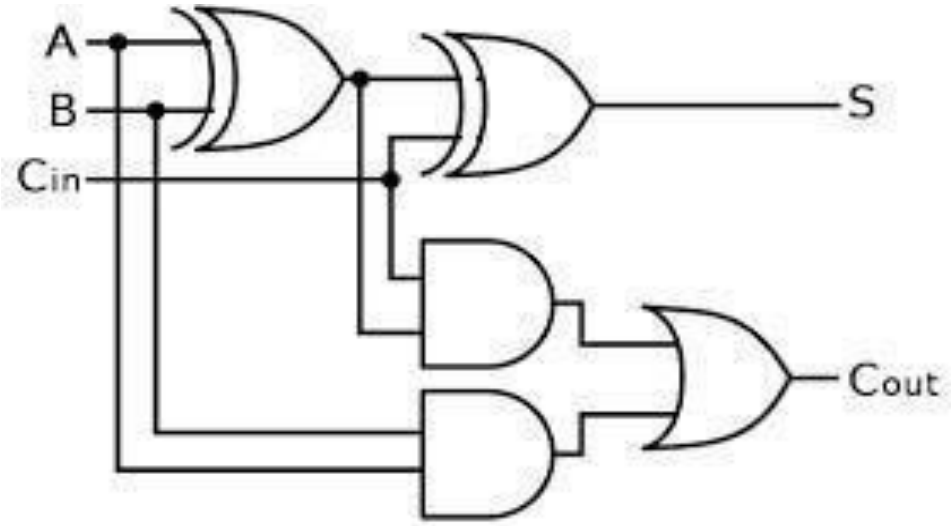
Truth Table:

A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

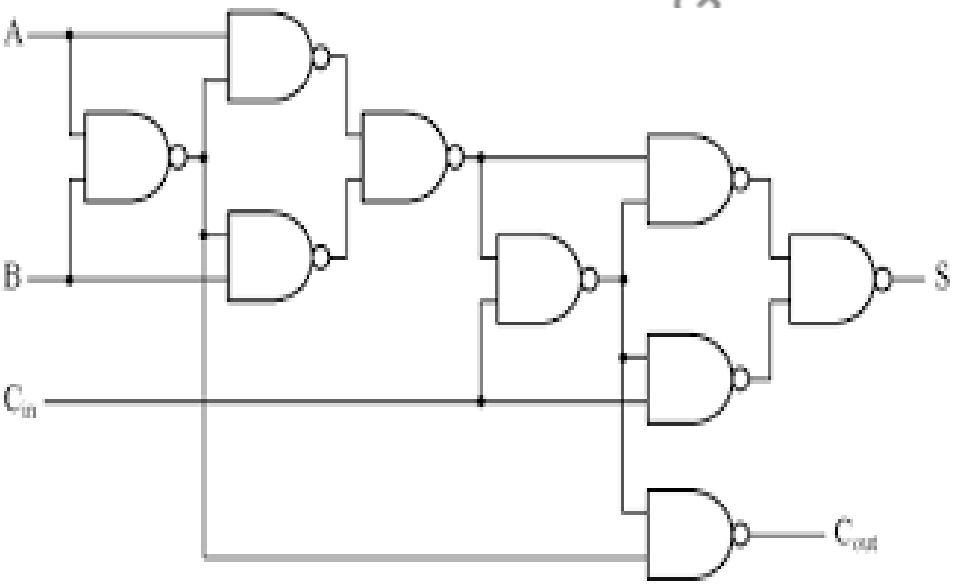
$S = A \oplus B \oplus C_{in}$

$C = A.B + C_{in} (A + B)$

Realization of Full Adder:



Using logic gates



Using NAND gates

3. Half Subtractor:

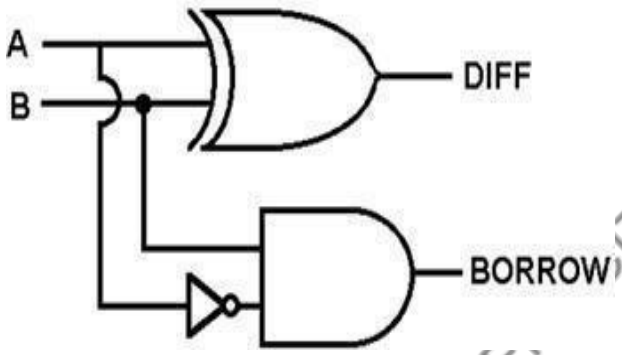
Truth Table:

A	B	D	Br
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D = A ⊕ B

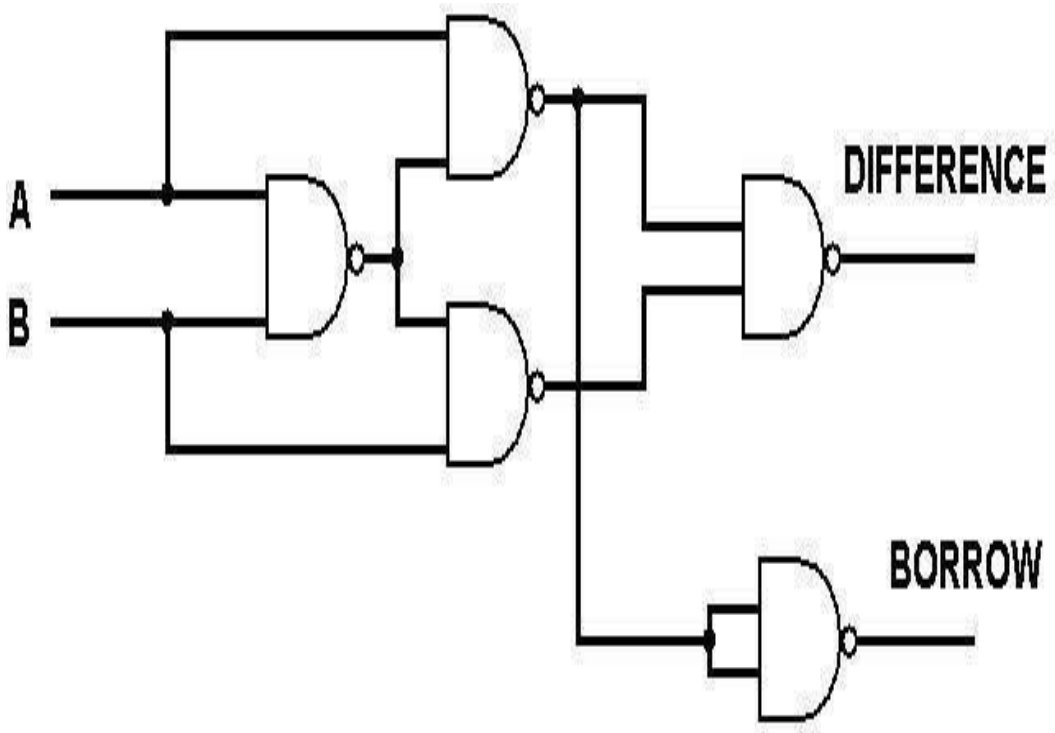
Br = A.B

Realization of Half Subtractor:



Using Logic Gates

Using NAND Gates



Full Subtractor:

Truth Table:

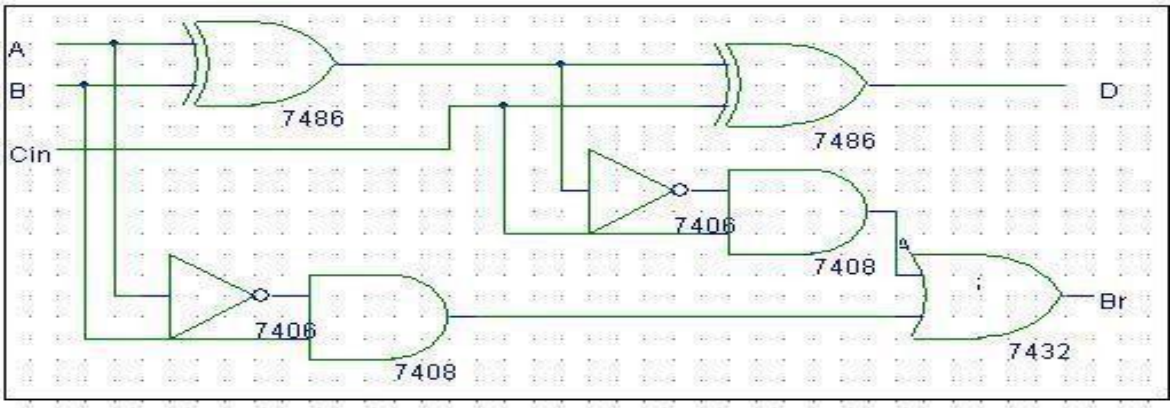
A	B	Cin	D	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = A \oplus B \oplus C_{in}$$

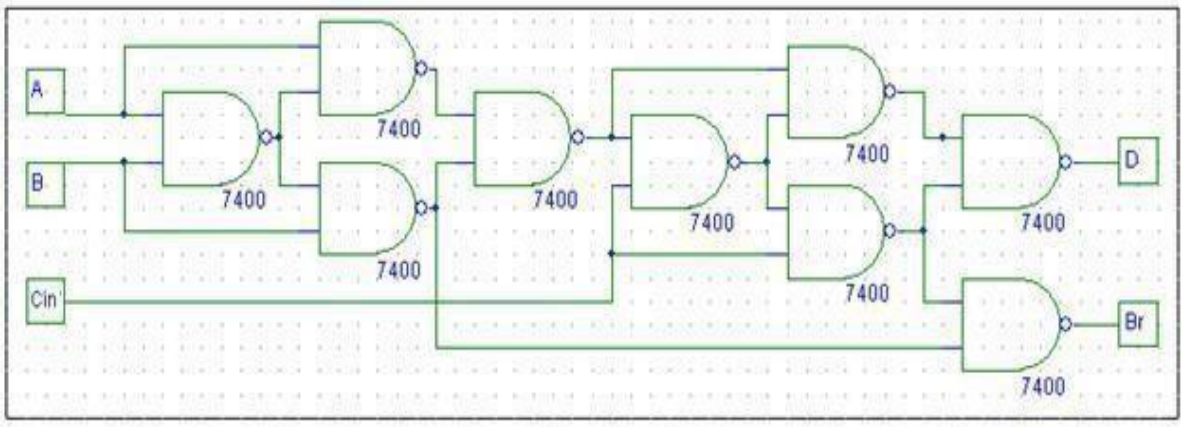
$$Br = A'.B + A'.C_{in} + B.C_{in}$$

Realization of Full Subtractor:

Using Basic gates



Using Basic gates



Using NAND gates

REALIZATION OF 4 VARIABLE FUNCTIONS USING IC 74151 (8:1 MUX)

Aim: To design and set up the following circuit using 4 variable function using IC 74151 (8:1 MUX)

Components Required: IC74151, Patch Cords & IC Trainer Kit.

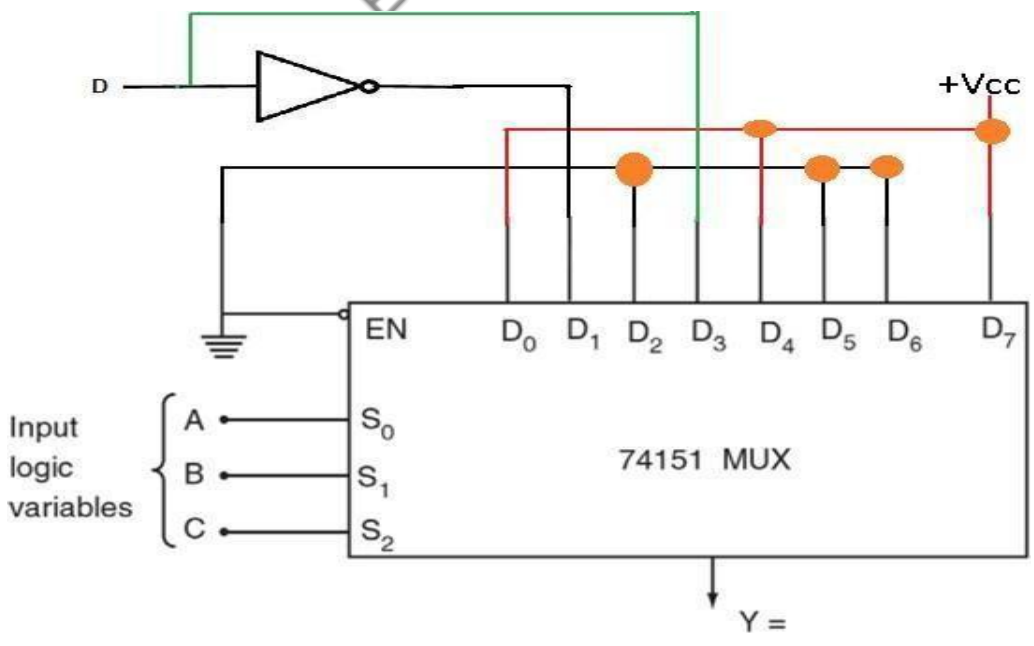
Theory:

Multiplexers are very useful components in digital systems. They transfer a large number of information units over a smaller number of channels, (usually one channel) under the control of selection signals.

Multiplexer means many to one. A multiplexer is a circuit with many inputs but only one output. By using control signals (select lines) we can select any input to the output. Multiplexer is also called as data selector because the output bit depends on the input data bit that is selected. The general multiplexer circuit has 2n input signals, n control/select signals and 1 output signal.

4 Variable function using IC 74151:

$Y = F(A,B,C,D) = \sum m(0,1,2,7,8,9,14,15$



Truth Table

ABC	000	001	010	011	100	101	110	111
D=0	1	1	0	0	1	0	0	1
D=1	1	0	0	1	1	0	0	1
Y	1	$\overline{D}$	0	D	1	0	0	1
8:1 MUX Data Input	$D_0 = 1$	$D_1 = \overline{D}$	$D_2 = 0$	$D_3 = D$	$D_4 = 1$	$D_5 = 0$	$D_6 = 0$	$D_7 = 1$

Procedure for Half Adder, Full Adder, Half Subtractor & Full Subtractor:

1. Verify that the gates are working.
2. Make the connections as per the circuit diagram for the half adder circuit, on the trainer kit.
3. Switch on the VCC power supply and apply the various combinationsof the inputs according to the respective truth tables.
4. Verify that the outputs are according to the expected results.
5. Repeat the procedure for the full adder circuit, the half subtractorand full subtractor circuits.
6. Verify that the sum/difference and carry/borrow bits are according tothe expected values.

Procedure for 8:1 MUX:

1. For the given expression, a truth table is to be written.
2. An expression in SOP format is to be written.
3. The connection is made according to the obtained expression.
4. The truth table is verified for that particular expression.

Result:

Experiment No: 6 **Date:**

(a) Binary to Gray code conversion and Vice-versa (IC 74139)

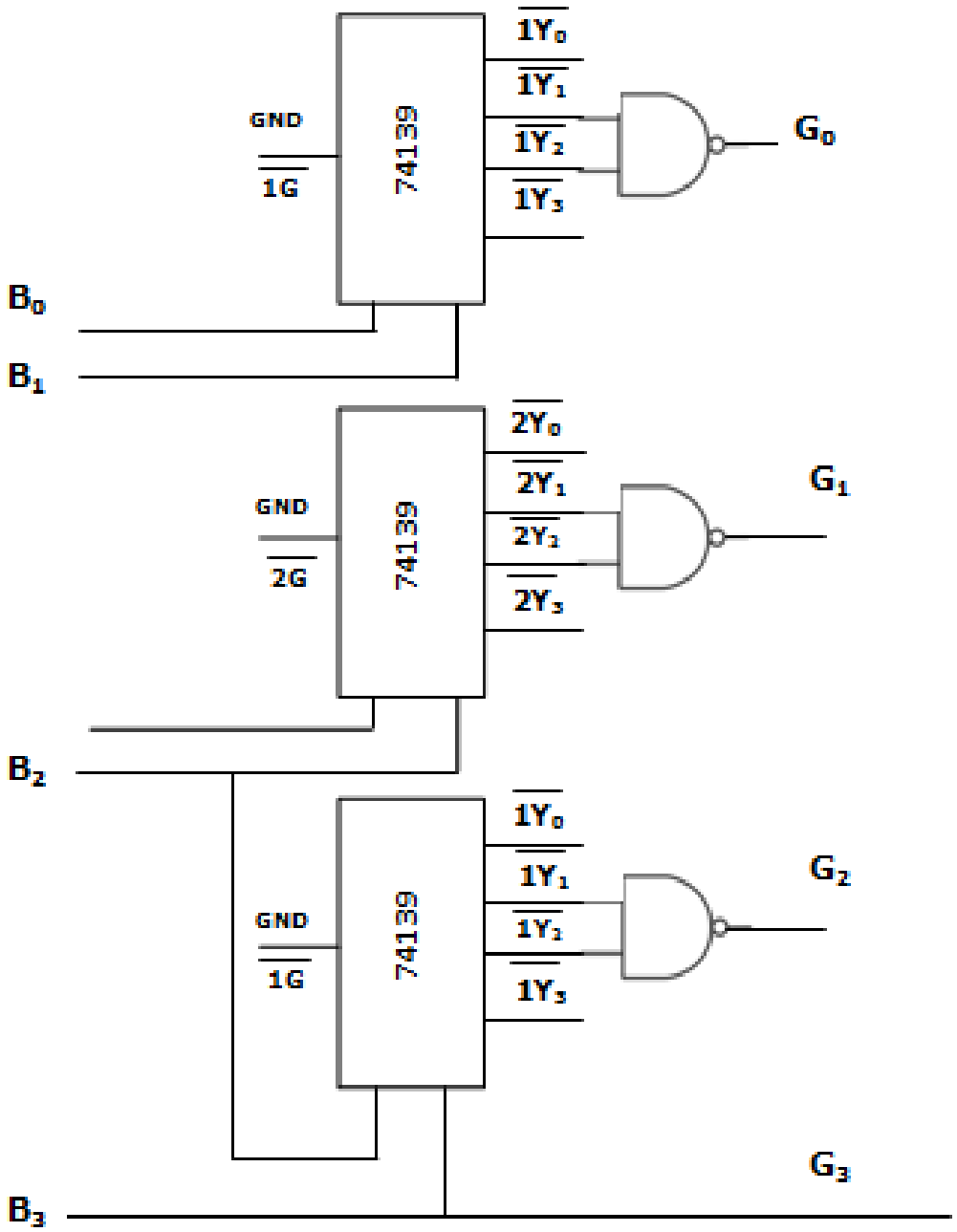
(b) BCD to Excess-3 code conversion and vice versa

Binary to Gray Conversion

Truth Table:

Binary Inputs				Gray Outputs			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

(i) Realization using74139:

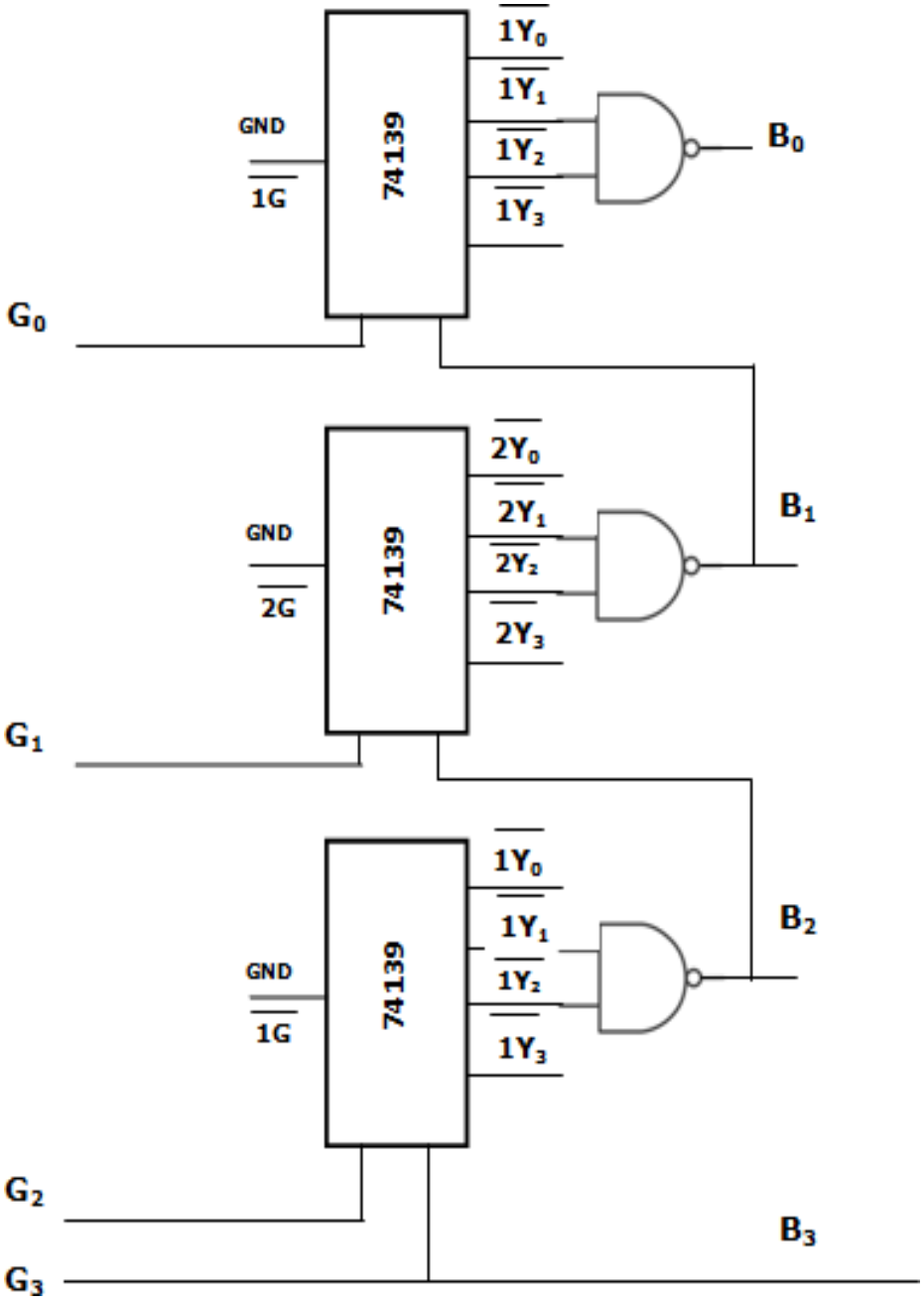


Gray to Binary Conversion:

Truth Table:

Gray Inputs				Binary Outputs			
G3	**G2**	**G1**	**G0**	**B3**	**B2**	**B1**	**B0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Realization using 74139:



BCD TO EXCESS-3 CODE CONVERTERS & VICEVERSA

Aim: To design and realize the following using IC7483.

(i) BCDtoExcess-3Code

(ii) Excess-3toBCDCode.

Components Required: IC7483 ,IC7486, Patch Cords & IC Trainer Kit.

Theory:

Code converter is a combinational circuit that translates the input code word into a new corresponding word. The excess-3 code digits obtained by adding three to the corresponding BCD digit. To Construct aBCD-to-excess-3-code converter with a 4-bit adder feed BCD code to the 4-bit adder as the first operand and then feed constant3 as the second operand. The output is the corresponding excess-3code.

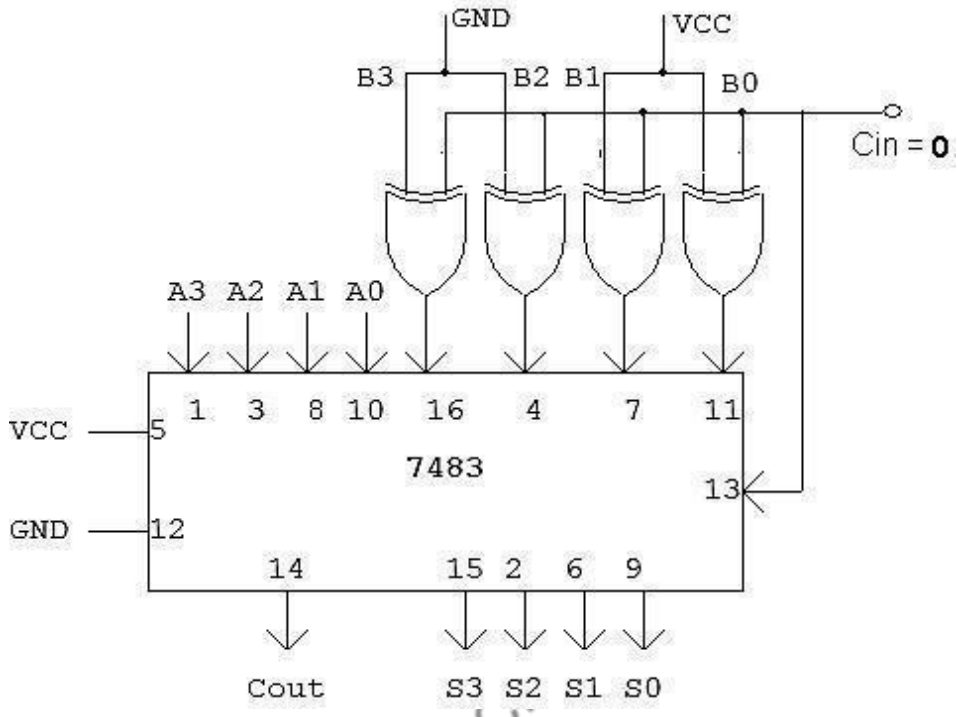
To make it work as aexcess-3 to BCD converter, we feed excess-3code as the first operand and then feed 2's complement of 3 as the second operand .The output is the BCD code.

(i) BCDtoExcess-3Code

Truth Table:

BCD Inputs				Excess3 outputs			
B3	**B2**	**B1**	**B0**	**E3**	**E2**	**E1**	**E0**
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Circuit:

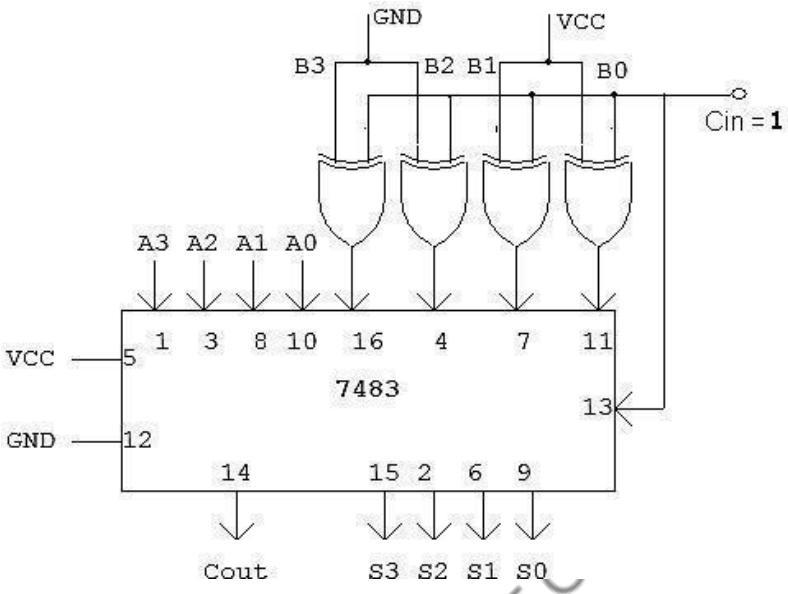


(ii) Excess-3-codetoBCD:

Truth Table:

Excess-3Inputs				BCD Outputs			
E3	**E2**	**E1**	**E0**	**B3**	**B2**	**B1**	**B0**
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

Circuit:



Procedure for BCD to Excess-3:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Apply BCD code as first operand (A) and binary3 as second operand (B)and C_{in}=0 for Realizing BCD-to-Excess-3-code:

Procedure for Excess-3 to BCD:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram..
4. Apply BCD code as first operand (A) and binary3 as second operand (B)and C_{in}=0 for Realizing BCD-to-Excess-3-code:

Result:

ExperimentNo : 7 **Date:**

FLIPFLOPS

Aim: To realize the following Flip Flops using NAND gates: Master slave JK, D and T Flip-flops.

Components required: IC7410, IC7400, PatchCords

Theory:

A flip-flop is a circuit that has two stable states and can be used to store state information. A flip-flop is a bi stable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

A flip–flop is a **"bit bucket"**; it holds a single binary bit .Flip flops are actually an application of logic gates. With the help of Boolean logic we can create memory with them. Flip flops can also be considered as the most basic idea of a Random Access Memory [RAM].

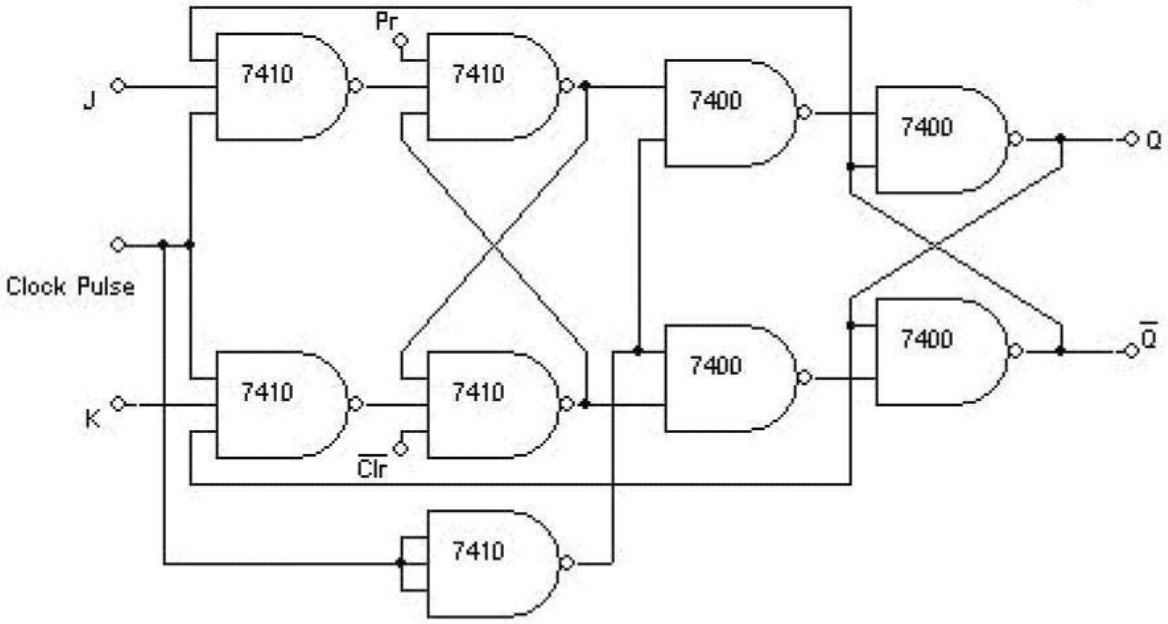
The most commonly use application of flip flops is in the implementation of a feedback circuit . As a memory relies on the feedback concept, flipflops can be used to design it.

J-K MASTER FLIPFLOP:

Truth Table:

$\overline{\text{Preset}}$	$\overline{\text{Clear}}$	J	K	Clock	Q_{n+1}	$\overline{Q_{n+1}}$	Status
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⎍	Q_n	$\overline{Q_n}$	No Change
1	1	0	1	⎍	0	1	Reset
1	1	1	0	⎍	1	0	Set
1	1	1	1	⎍	$\overline{Q_n}$	Q_n	Toggle

Circuit:

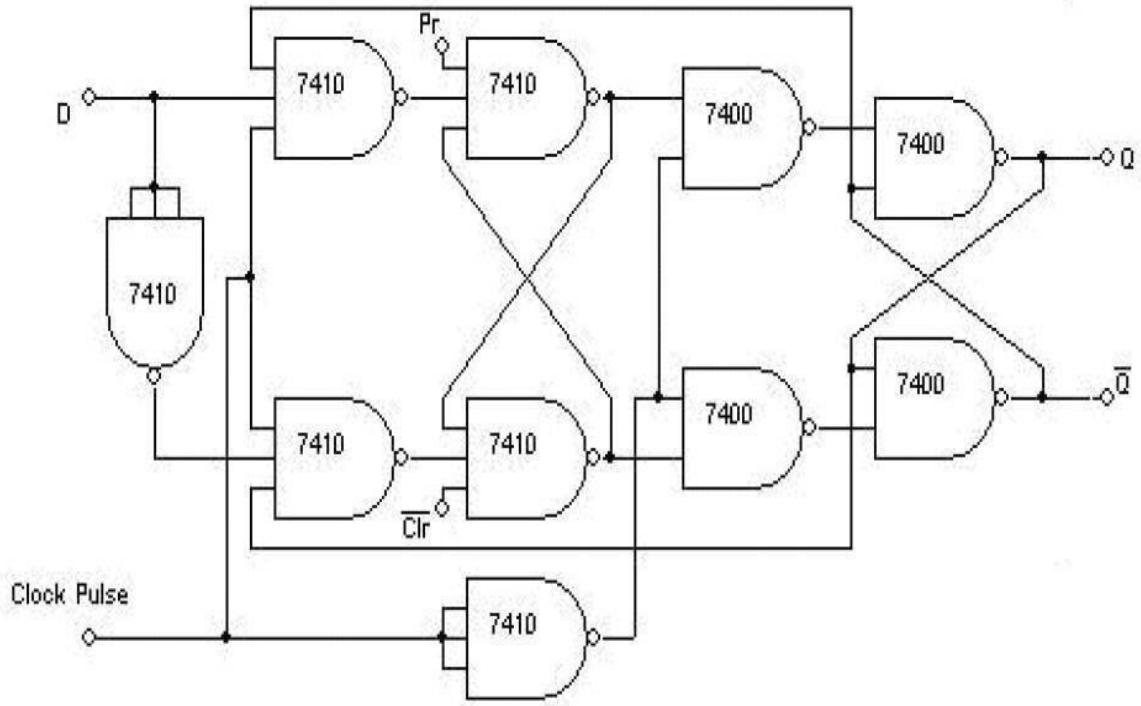


D–FLIPFLOP:

Truth Table:

$\overline{\text{Preset}}$	$\overline{\text{Clear}}$	D	Clock	Q_{n+1}	$\overline{Q_{n+1}}$
1	1	0	⎍	0	1
1	1	1	⎍	1	0

Circuit:

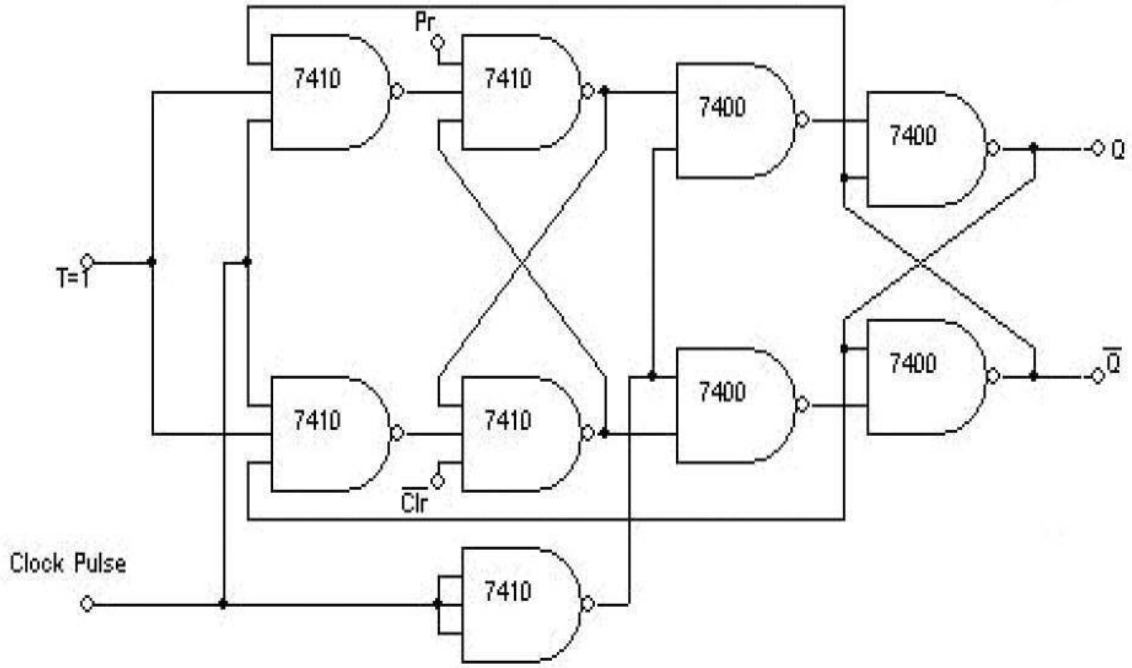


T–FLIPFLOP:

TruthTable:

$\overline{\text{Preset}}$	$\overline{\text{Clear}}$	T	Clock	Q_{n+1}	$\overline{Q_{n+1}}$
1	1	0	⎍	Q_n	$\overline{Q_n}$
1	1	1	⎍	$\overline{Q_n}$	Q_n

Circuit:



Procedure:

1. Make the connections as shown in the circuit diagrams.
2. Apply inputs as shown in the truth tables,
3. Check the outputs of the circuits ;verify that the ymatch with the truth tables.

Result:

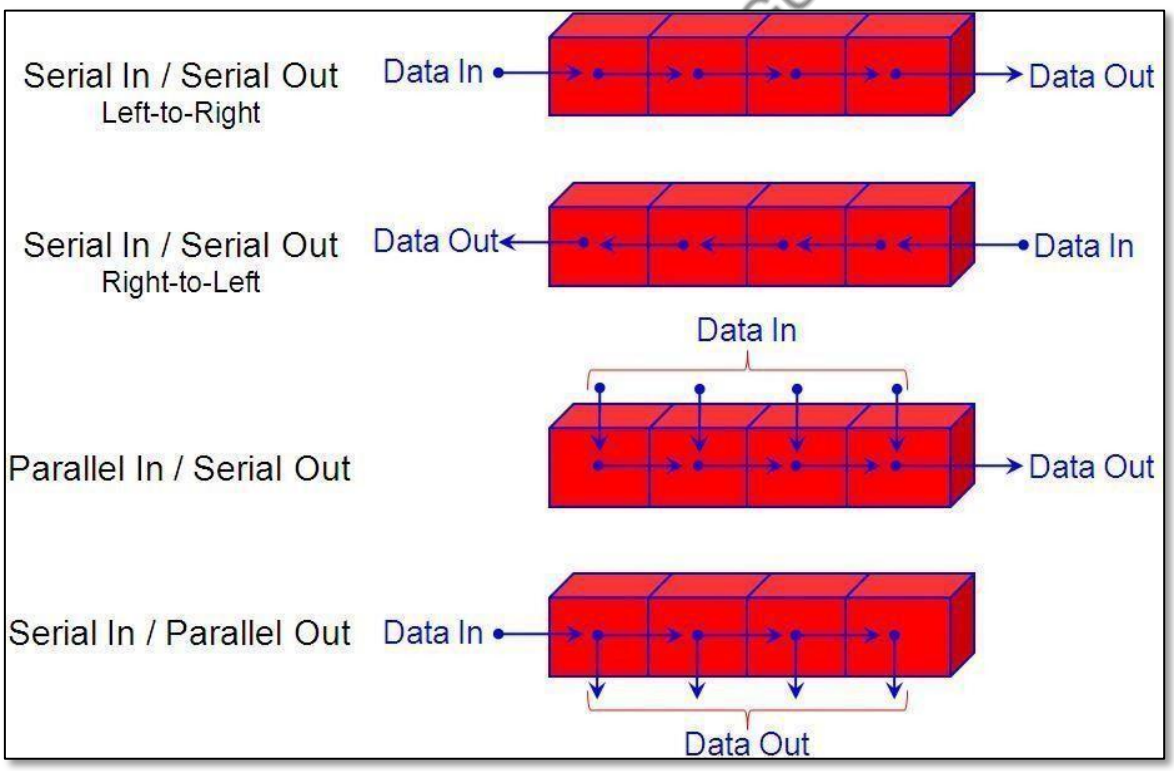
SHIFT REGISTERS

Aim: To study IC74S95, and the realization of Shift left, Shift right, SIPO, SISO, PISO, PIPO operations using the same.

Components required:IC7495,patchcords etc.

Theory:

- A shift register is a group of flip-flops (typically4 or 8) that are arranged so that the values stored in the flip-flops are shifted from one flip-flop to the next for every clock.
- Shift registers are used extensively in logic circuits to control digital displays.
- A classic example is numbers being typed into a calculator. As the numbers are entered, the digits shift to the left one position. This shifting is controlled by a shift register.



SERIAL INPUT SERIAL OUTPUT (SISO) Procedure:

1. Connections are made as shown in the SISO circuit diagram.

2. Make sure the 7495 is operating in SISO mode by ensuring Pin6 (Mode) is set to LOW, and connect clock input to Clk1 (Pin9).

3. The shift register is loaded with 4 bits of data one by one serially.

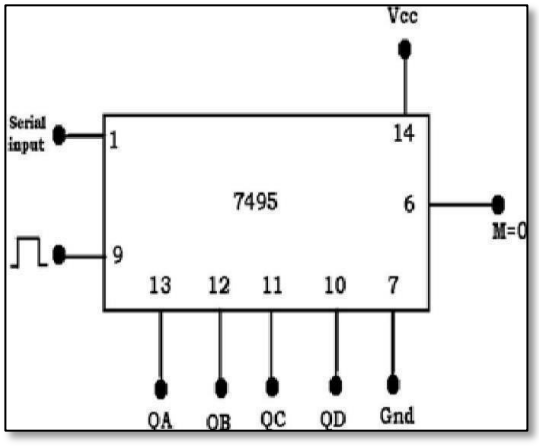
4. At the end of the 4th clock pulse, the first data'd0'appears at QD.

5. Apply another clock pulse, to get the second data bit, 'd1' at QD. Applying yet another clock pulse gets the third data bit,'d2 'at QD, and soon.

TruthTable:

CLK	Serial I/P	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

CircuitDiagram:



SERIAL INPUT PARALLEL OUTPUT (SIPO/Right Shift) Procedure:

1. Connections are made as shown in the SISO circuit diagram.

2. Make sure the 7495 is operating in SIPO mode by ensuring Pin 6 (Mode) is set to LOW ,and connect clock input to Clk1(Pin9).

3. Apply the first data at pin 1 (SD1) and apply one clock pulse. We observe that this data appears at pin13(QA).

4. Now, apply the second data at SD1. Apply a clock pulse. We now observe that the earlier data is shifted from QA to QB, and the new data appears at QA.

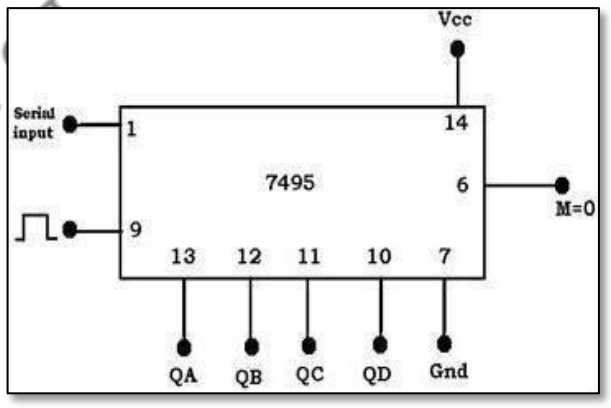
5. Repeat the earlier s tep to enter data ,until all bits are entered one by one.

6. At the end of the 4th clock pulse, we notice that all 4 bits are available at the parallel output pins QA through QD.

Truth Table:

CLK	Serial I/P	QA	QB	QC	QD
1	1	1	X	X	X
2	0	0	1	X	X
3	1	1	0	1	X
4	1	1	1	0	1

Circuit:



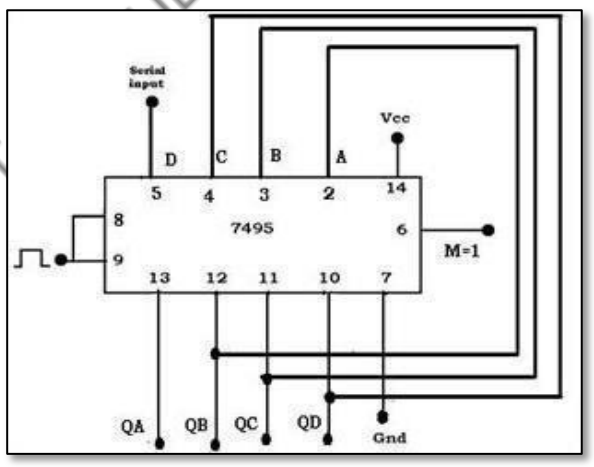
SERIAL INPUT PARALLEL OUTPUT (SIPO/Left Shift) Procedure*:*

1. Connections are made as shown in the SISO circuit diagram.
2. Make sure the 7495 is operating in Parallel mode by ensuring Pin 6 (Mode)is set to HIGH, and connect clock input to Clk2 (Pin8).
3. Apply the first data at pin5(D) and apply one clock pulse .We observe that this data appears at pin10 (QD).
4. Now, apply the second data at D .Apply a clock pulse. observe that the earlier data is shifted from QD to QC, and the new data appears at QD.
5. Repeat the earlier step to enter data, until all bits are entered one by one.
6. At the end of the 4thclockpulse, we notice the tall4bits are available at the parallel output pins QA (MSB), QB, QC, QD (LSB).

Truth Table:

CLK	Serial I/P	QA	QB	QC	QD
1	1	X	X	X	1
2	0	X	X	1	0
3	1	X	1	0	1
4	1	1	0	1	1

Circuit:



PARALLEL INPUT PARALLEL OUTPUT (PIPO):

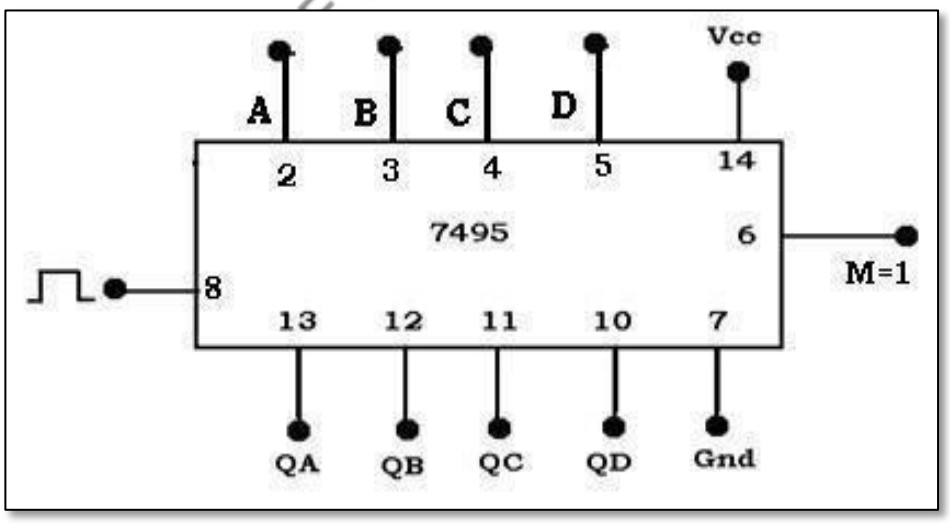
Procedure:

1. Connections are made as shown in the SISO circuit diagram.
1. Set Mode Control M to HIGH to enable Parallel transfer.
2. Apply the 4databits as input to pins A,B,C,D.
3. Apply one clock pulse a tClk2 (Pin8).
4. Note that the 4bit data at parallel inputs A,B,C,D appears at the parallel output pins Q , QB, QC ,QD respectively.

Truth Table:

	ParallelI/P				ParallelO/P			
CLK	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

Circuit:



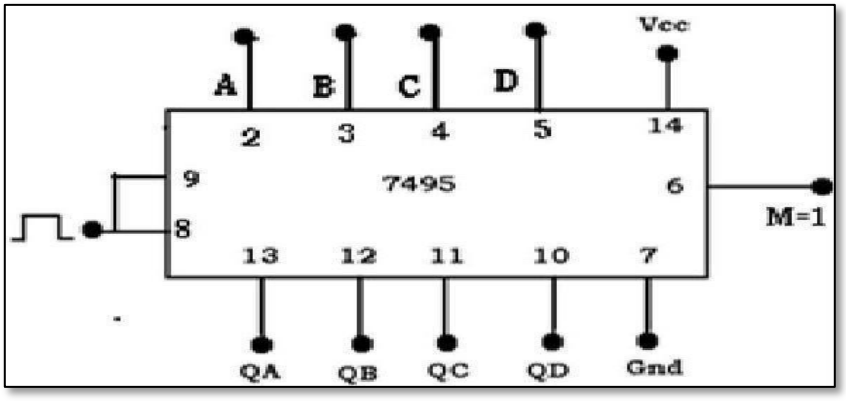
PARALLEL INPUT SERIAL OUTPUT (PISO) Procedure:

1. Connections are made as shown in the SISO circuit diagram.
2. Now apply the 4-bit data at the parallel I/P pins A, B,C,D (pins2through5).
3. Keeping the mode control M on HIGH, apply one clock pulse. The data applied at the parallel input pins A, B, C, D will appear at the parallel output pins QA, QB, QC, QD respectively.
4. Now set the Mode Control M to LOW, and apply clock pulses one by one. Observe the data coming out in a serial mode at QD.
5. We observe now that the IC operates in PISO mode with parallel inputs being transferred to the outputs serially.

TruthTable:

Mode	Clock	ParallelI/P				O/P			
M	**CLK**	**A**	**B**	**C**	**D**	**QA**	**QB**	**QC**	**QD**
1	1	**1**	**0**	**1**	**1**	1	0	1	**1**
0	2	X	X	X	X	X	1	0	**1**
0	3	X	X	X	X	X	X	1	**0**
0	4	X	X	X	X	X	X	X	**1**

Circuit:

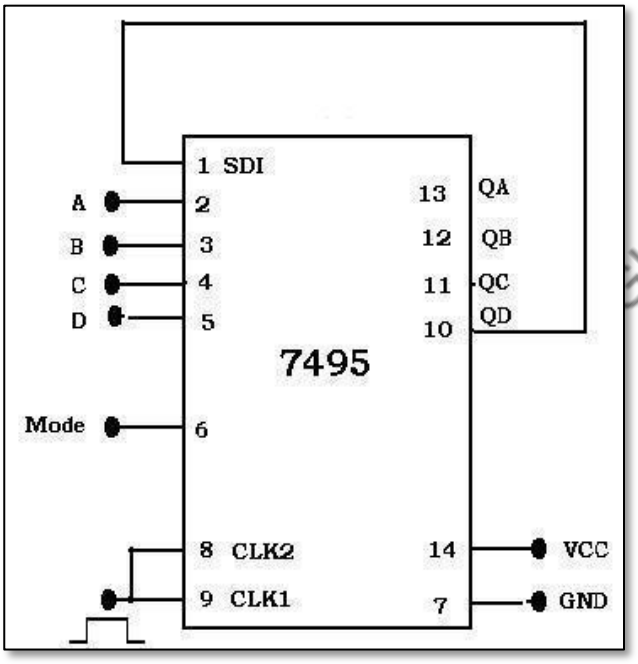


Ring counter:

Truth Table:

M	CLK	QA	QB	QC	QD
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	0	1	0	0

Circuit:

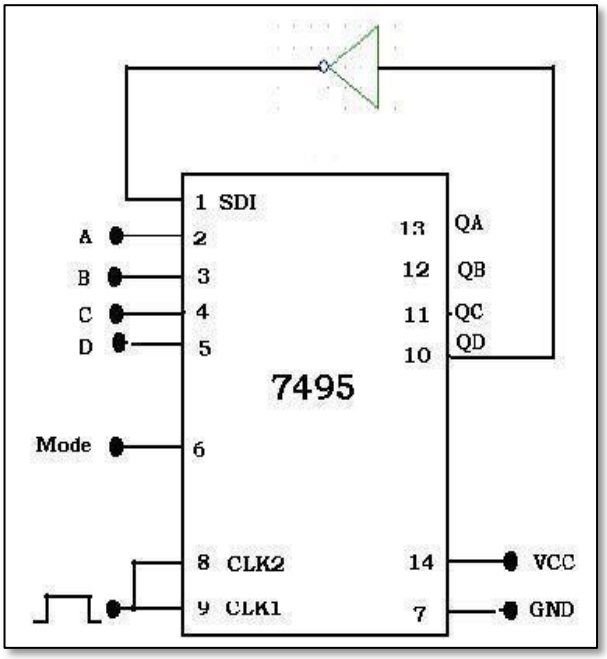


JHONSON Counter:

Truth Table:

M	CLK	QA	QB	QC	QD
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	1	1	0	0

Circuit:



Theory:

A ***ring counter*** is a circular shift register which is initiated such that only one of its flip-flops is the state one while others are in their zero states.

A ring counter is a Shift Register with the output of the last one connected to the input of the first, that is, in a ring. Typically, a pattern consisting of a single bit is circulated so the state repeats every n clock cycles if n flip-flops are used .It can be used as a cycle counter of n states.

A ***Johnson counter*** (or switch tail ring counter, twisted-ring counter, walking-ring counter, or Moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. The register cycles through a sequence of bit-patterns, whose length is equal to twice the length of the shift register, continuing indefinitely. These counters find specialist applications, including those similar to the decade counter, digital-to-analog conversion, etc. They can be implemented easily using D-or JK-type flip-flops.

Procedure:

1. Make the connections as shown in the respective circuit diagram.
2. Initial condition is set by setting up the circuit as shown in the figure.
3. There after all Prand Clr pins of all F/Fs should be connected to VCC.
4. Apply clock and observe the output after reach clock pulse, record the observations and verify that they match the expected outputs from the truth table.
5. Repeat the same procedure as above for the Johnson Counter circuit and verify its operation

Result:

ExperimentNo :8 **Date:**

MOD N SYNCHRONOUS UP/DOWNCOUNTER USING 7476

Aim: To design and test3 –bit binary synchronous counter using flip-flopIC7476forthegivensequence.

Components Required: IC7476,PatchCords&ICTrainerKit

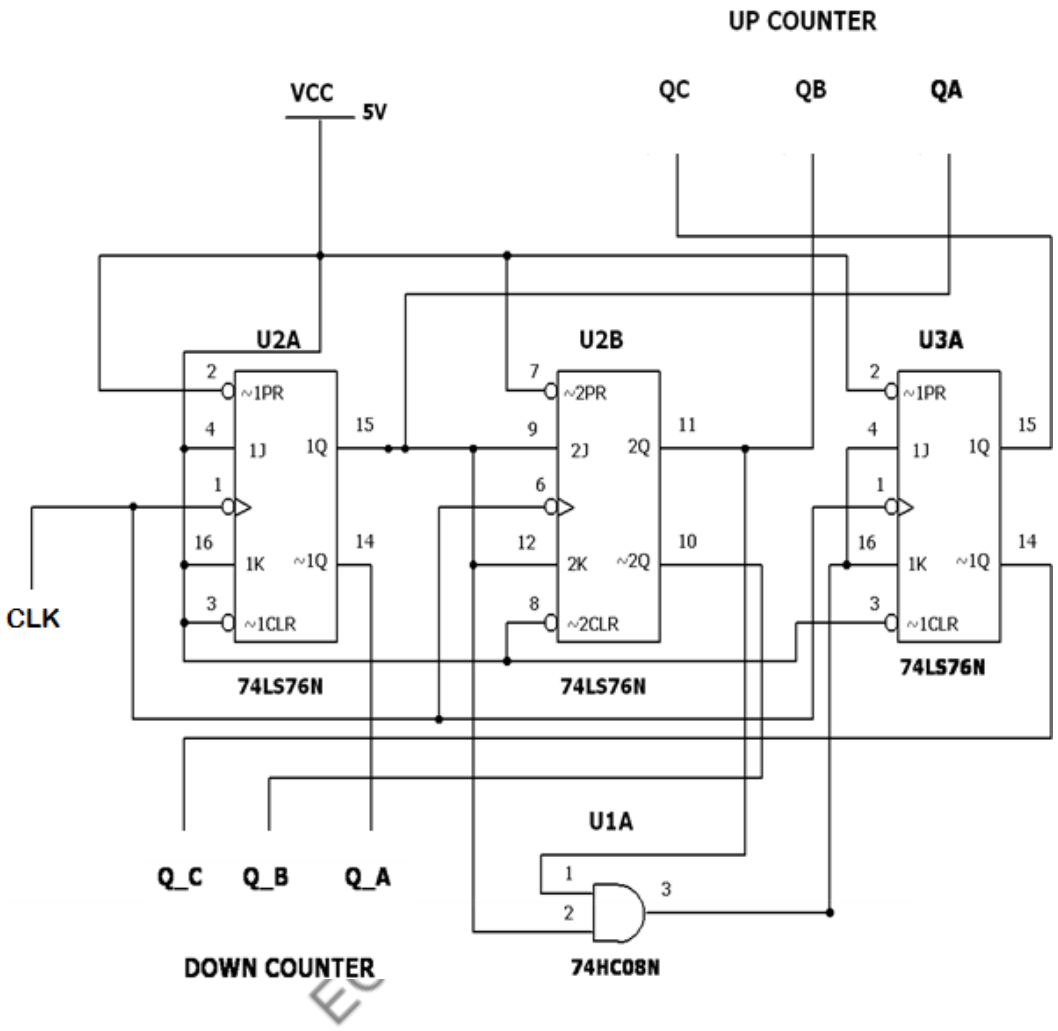
Theory:

A counter in which each flip-flop is triggered by the output goes to previous flip-flop. As all the flip-flops do not change state s simultaneously in asynchronous counter, spike occur at the output. To avoid this, strobe pulse is required .Because of the propagation delay the operating speed of asynchronous counter is low. This problem can be solved by triggering all the flip-flops in synchronous with the clock signal and such counters are called synchronous counters.

Procedure:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

MOD8 UP and DOWN COUNTER:



Truth Table:

CLK	UPCOUNTER			DOWNCOUNTER		
	QC	QB	QA	QC	QB	QA
0	0	0	0	1	1	1
1	0	0	1	1	1	0
2	0	1	0	1	0	1
3	0	1	1	1	0	0
4	1	0	0	0	1	1
5	1	0	1	0	1	0
6	1	1	0	0	0	1
7	1	1	1	0	0	0

REALIZE MOD N ASYNCHRONOUS COUNTER USING IC7490

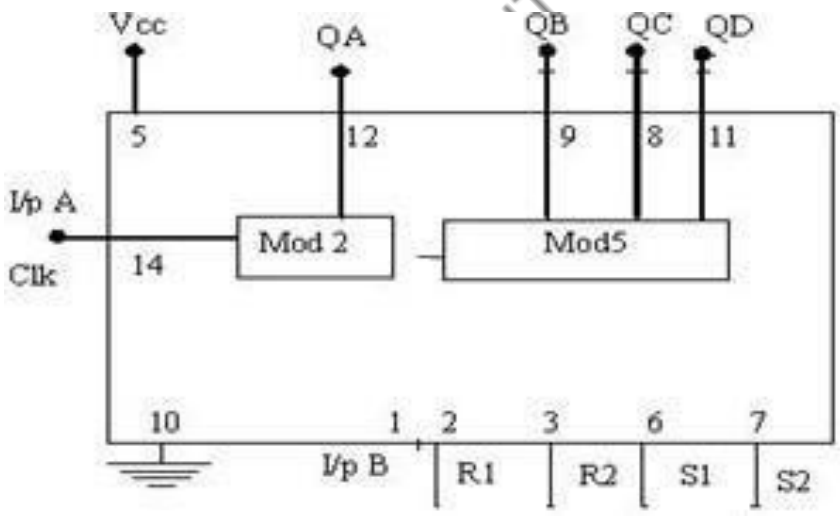
Aim: To rig up Mod N asynchronous counter using IC7490 and synchronous counter using IC74192.

Components required: IC7490, Patch cords, trainer kit, etc.

Procedure:

1. Check all the components for their working.
2. Make connections as shown in the circuit diagram.
3. Clock pulses are applied one by one at the clock input and output is observed at QA ,QB, QC and QD
4. Verify the Truth Table and observe the outputs.

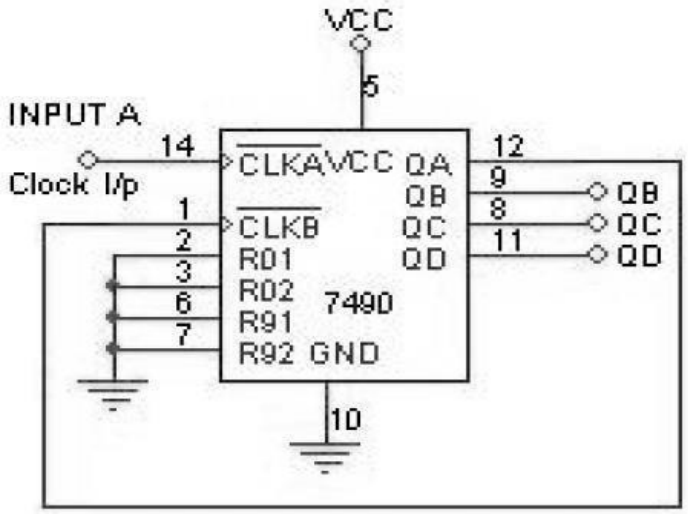
Note: Internal block diagram of IC 7490



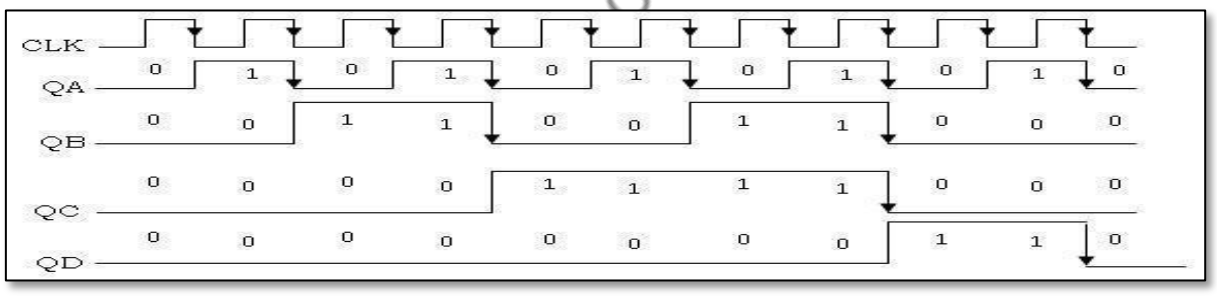
MOD10 Asynchronous Counter:

Truth Table:

CLK	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1



Waveforms:



REALIZE MOD N SYNCHRONOUS COUNTER USING IC74192

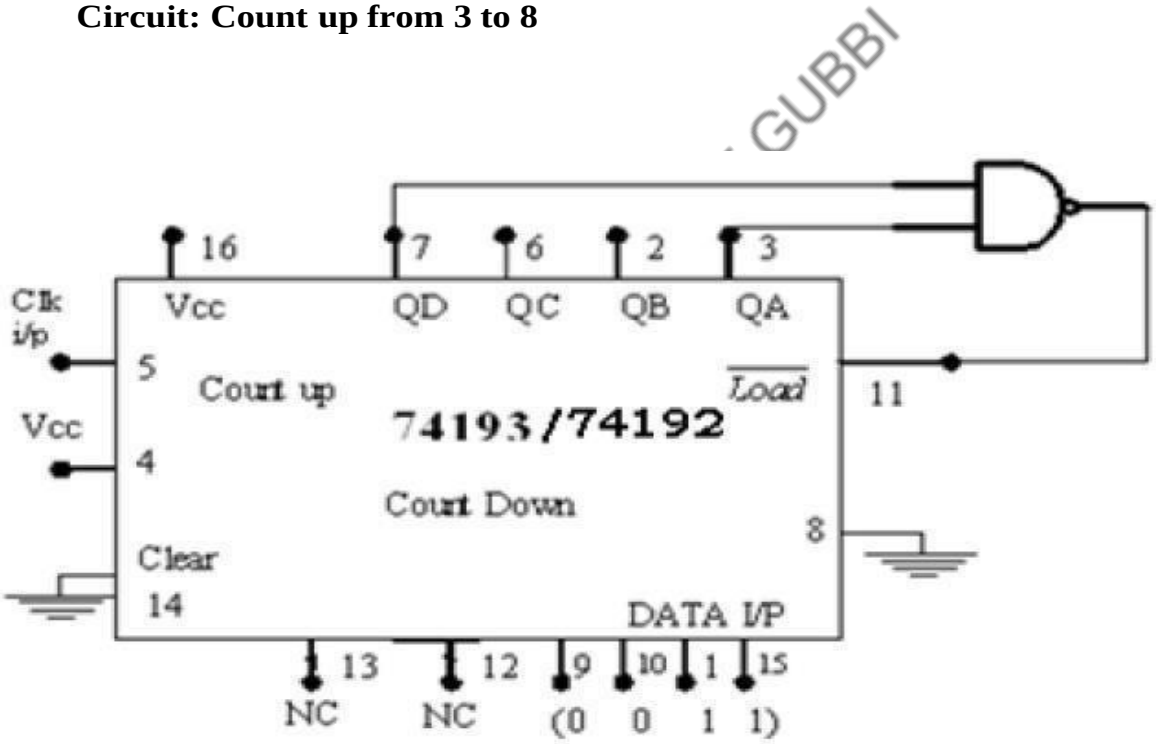
Aim: To rigup ModN asynchronous counter using IC74192.

Components required: IC7490, Patch cords, trainer kit, etc.

Procedure:

1. Check all the components for their working.
2. Make connections as shown in the circuit diagram.
3. Clock pulses are applied one by one a t the clock input and output is observed at QA,QB,QC and QD
4. Verify the Truth Table and observe the outputs.

Circuit: Count up from 3 to 8



Truth Table:

Clk	QD	QC	QB	QA
0	0	0	1	1
1	0	1	0	0
2	0	1	0	1
3	0	1	1	0
4	0	1	1	1
5	1	0	0	0
6	0	0	1	1

Result:

DEMONSTRATION EXPERIMENTS

Experiment No. 9(a) **Date:**

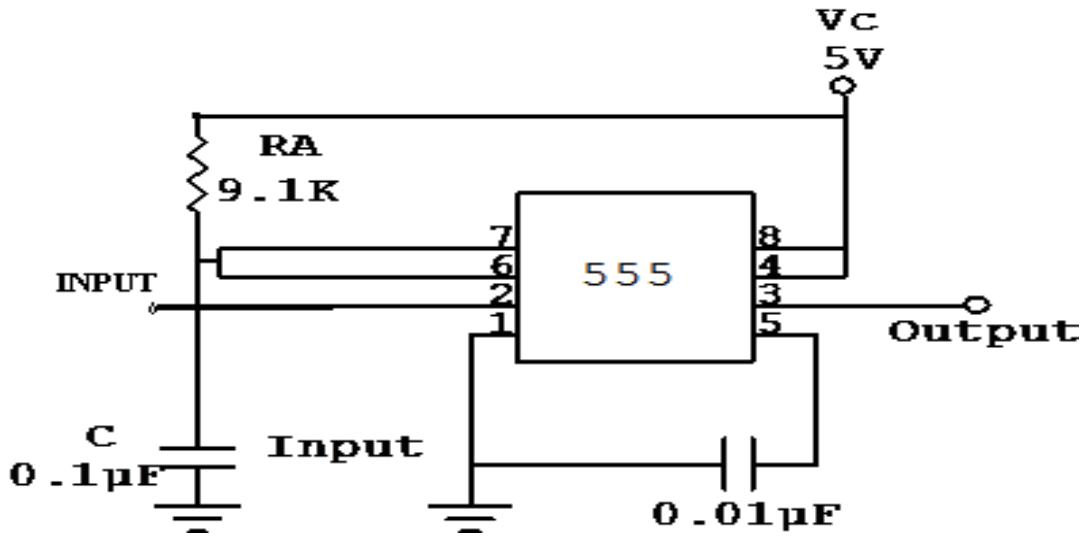
MONOSTABLE MULTIVIBRATOR

AIM: To design and study the Monostable Multivibrator circuit using 555 timer.

APPARATUS:

Name	Description	Qty
IC-555	-	1
Resistors	9.1 KΩ	1
Capacitors	0.1 µF 0.01 µF	1 1
Digital Trainer Kit	-	1
Patch Cords	-	-

CIRCUIT DIAGRAM:



DESIGN:

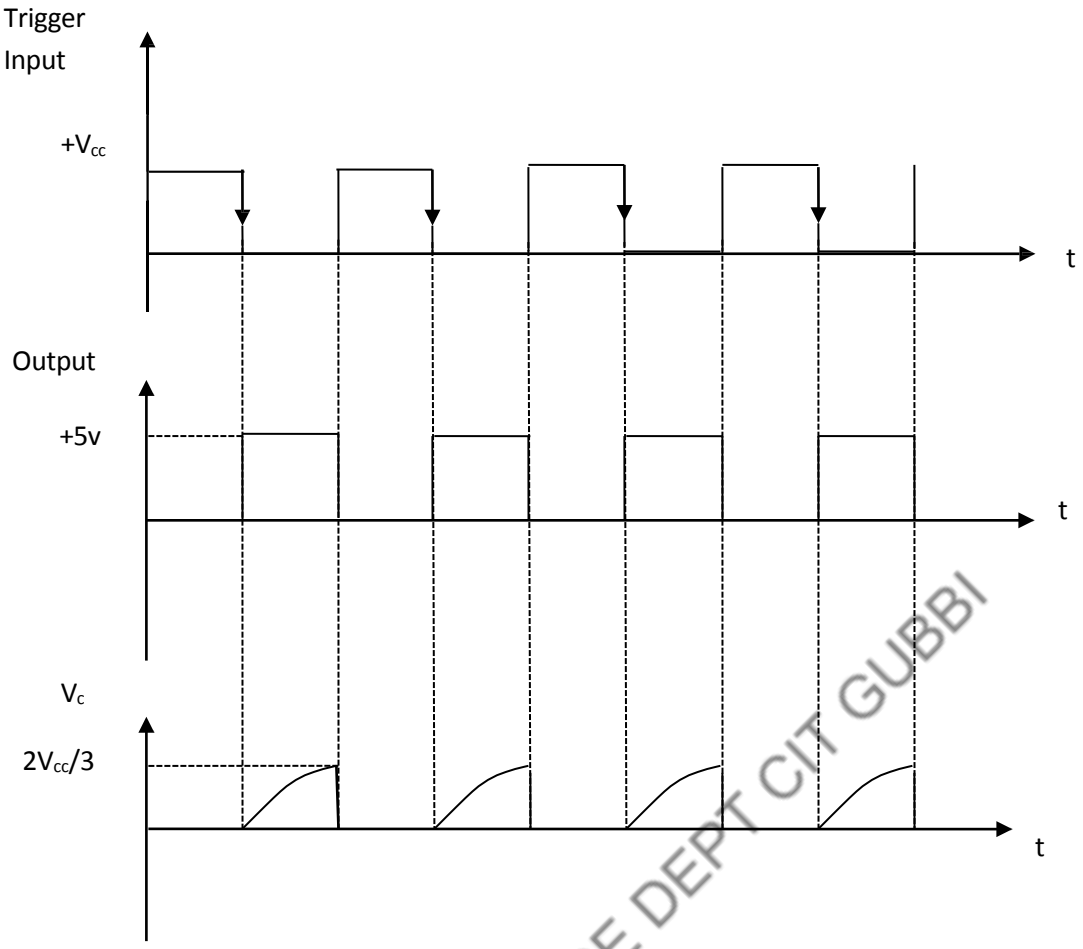
Let the time for which output remaining high, T_p= 1 ms

T_p= 1.1R_AC, where C=0.1µF. Compute R_A

PROCEDURE:

1. Connect the circuit as shown above.
2. Give a trigger input to pin 2 and observe the output at pin 3.
3. Observe the charging and discharging waveforms across 0.1 µF.
4. Note down the value of 2Vcc/3.
5. Verify the charging period and the ON period for which it is designed

EXPECTED WAVEFORMS:



RESULT:

	Theoretical Value	Practical value
T_p		
V_{cc}		
2 $V_{cc}/3$		

Experiment No. 9 (b) **Date:**

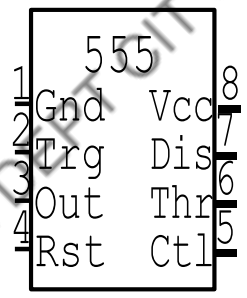
ASTABLE MULTIVIBRATOR

AIM: To design and study the Astable Multivibrator circuit using 555 timer.

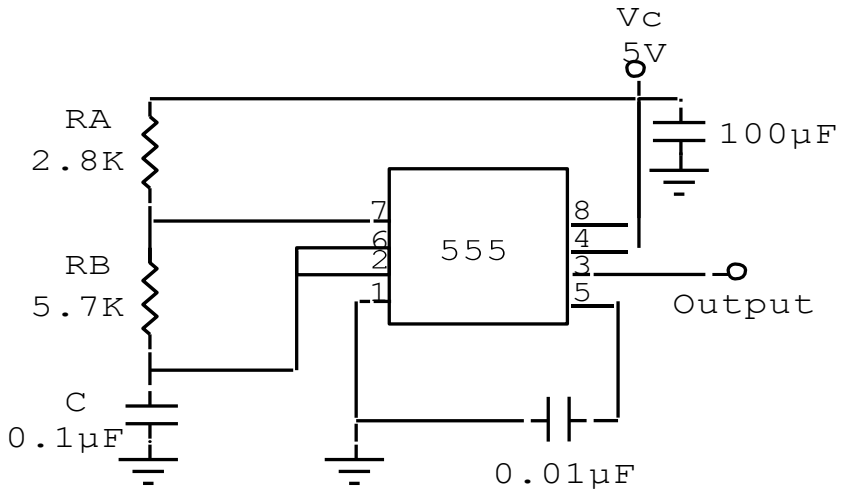
APPARATUS:

Name	Description	Qty
IC-555	-	1
Resistors	2.8 K, 5.7 K, 7.2 K	1 each
Capacitors	100 µF, 0.1 µF, 0.01 µF	1 each
Diode	IN4001	1
Digital Trainer Kit	-	1
Patch cords	-	-

CIRCUIT DIAGRAM:



a. ASYMMETRIC ASTABLE MULTIVIBRATOR:



DESIGN:

Assume Frequency = 1 kHz and Duty Cycle = 60%

$T = T_{ON} + T_{OFF} = 1$ ms

Duty Cycle= $\frac{T_{ON}}{T_{ON} + T_{OFF}} = 0.6$

Compute T_{ON} and T_{OFF}

$T_{ON} = 0.693(R_A + R_B)C$

$T_{OFF} = 0.693R_BC$

Choose $C = 0.1\mu F$

Compute R_A and R_B

Result:

Experiment No. 10 **Date**:

II – Order Low Pass and High Pass Active Filters

Aim: Design a second order Butterworth active low pass / high pass filter for a given cut-off frequency. Conduct an experiment to draw frequency response and verify theroll off.

Apparatus Required:

Sl.No.	Particulars	Range	Quantity
1.	Op-amp µA741	-	01
2.	Resistors & Capacitors	As per design	-
3.	Probes	-	01 set

PROCEDURE:

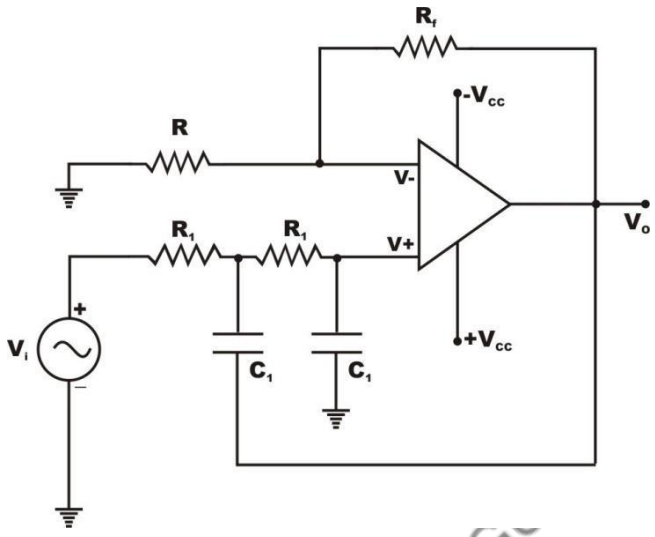
1. Connections are made as shown in the circuit diagram.
2. Apply sine wave i/p signal of peak amplitude 5 volts.
3. Check the gain of non-inverting amplifier by keeping the frequency of the input signalin the pass band of the filter. Note down the output voltage V_O max.
4. Keeping the input signal amplitude constant, vary the frequency until the outputvoltage reduces to 0.707 V_O max, the corresponding frequency is the cut-off frequency (f_C) of the filter.

To find the Roll-off factor:

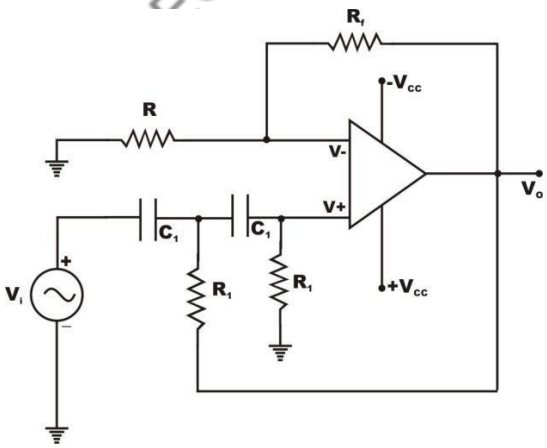
1. For LPF :- Keeping the input signal amplitude constant, adjust the input frequency at $10f_C$. Note down the output signal amplitude. The difference in the gain of the filter at f_C and $10f_C$ gives the Roll-of factor.
2. For HPF :- Keeping the input signal amplitude constant, adjust the input frequency at $0.1f_C$, note down the output signal amplitude. The difference in the gain of the filter at f_C and $0.1f_C$ gives the Roll-of factor.

CIRCUIT DIAGRAM:

II-Order Active Low Pass Filter



II- Order Active High Pass Filter



Design:- (LPF & HPF)

Assume Pass band gain AV = 2, Cutoff frequency f_C = 5KHz

1. **Amplifier: $A_V = 1 + \frac{R_f}{R} = 2$, then Rf = R, choose Rf = R = 10KΩ**

2. **Filter Circuit : Cut off frequency $f_C = \frac{1}{2\Pi R C_1} = 5$**

Choose C_1 = 0.01uf then R_1 = 3.183 KΩ

R_f = 10KΩ, R_1=3.3KΩ,

C_1 =0.01 f,

Op-amp = A741

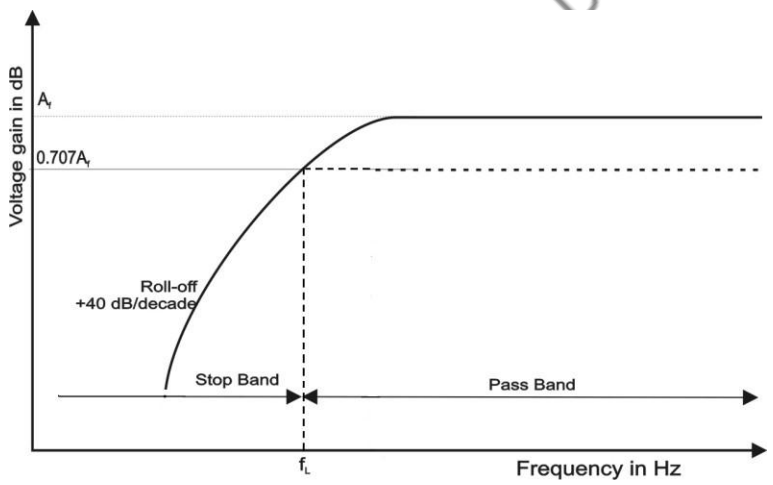
Tabulation:

High Pass Filter **Vi p-p =_____ Volts (Constant)**

I/P frequency in Hz	O/P Voltage VO P- P (volts)	Gain magnitude (Vo/Vi)	Gain magnitude in DB 20log(Vo/Vi)

Roll off = - (G1 - G2) db/decade =

Note: The values of G1, G2 are determined from the Tabular Column over a frequency rangeof 1 Decade.



Tabulation:

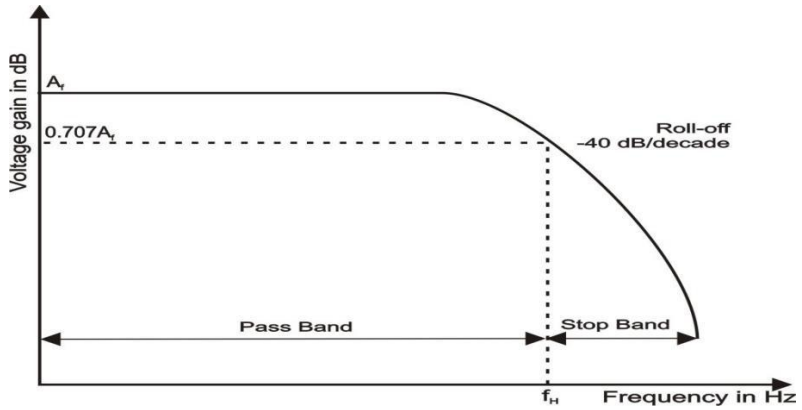
Low Pass Filter **Vi p-p = Volts (Constant)**

I/P frequency in Hz	O/P Voltage VO P- P (volts)	Gain magnitude (Vo/Vi)	Gain magnitude in DB 20log(Vo/Vi)

Roll off = - (G1 - G2) db/decade =

Note: The values of G1, G2 are determined from the Tabular Column over a frequency rangeof 1 Decade.

Frequency Response for Low Pass Filter



Experiment No. 11 **Date**:

DESIGN AND TEST REGULATED POWER SUPPLY

EQUIPMENT AND COMPONENTS USED

30 MHz Dual Channel Cathode Ray Oscilloscope

3 MHz Function Generator

0-30 V dc dual regulated power supply

4 ½ digit Digital Multimeter

230 V/ 9 V, 1A Step down transformer

1N4007 Diode

IC 7805

Resistor 100Ω, ¼W

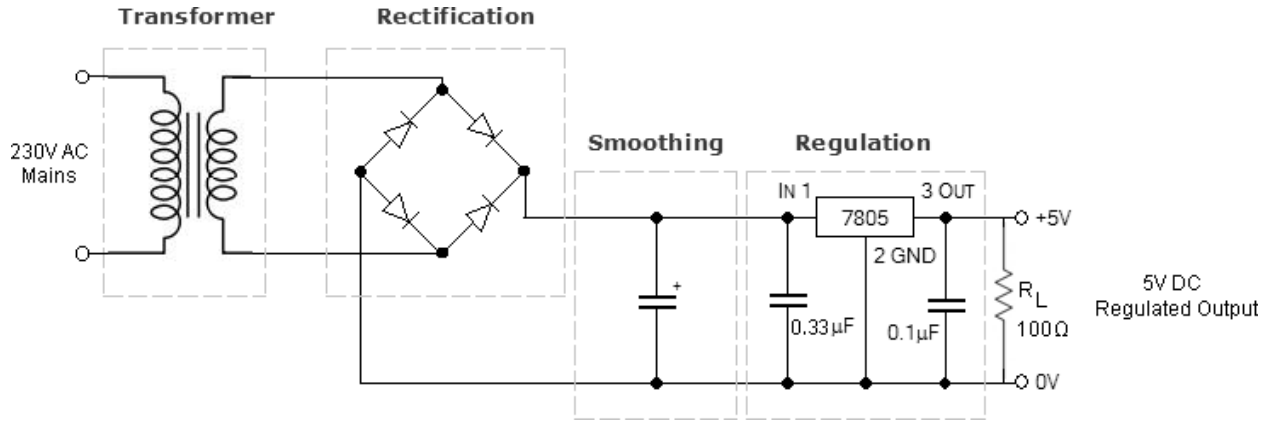
Electrolytic Capacitor 1000µF/25V

Ceramic Capacitor 0.33µF, 0.1 µF

Breadboard and Connecting wires BNC

Cables and Probes

CIRCUIT DIAGRAM:



Procedure:

1. Connect the circuit as shown in Figure 2.
2. Apply 230V AC from the mains supply.
3. Observe the following waveforms using oscilloscope
   (i) Waveform at the secondary of the transformer
   (ii) Waveform after rectification
   (iii) Waveform after filter capacitor
   (iv) Regulated DC output

DESIGN

Design a 5 V DC regulated power supply to deliver up to 1A of current to the load with 5% ripple. Theinput supply is 50Hz at 230 V AC.

Selection of Voltage regulator IC:

Fixed voltage linear IC regulators are available in a variation of voltages ranging from -24V to +24V. The current handling capacity of these ICs ranges from 0.1A to 3A. Positive fixed voltage regulator ICs have the part number as 78XX.

The design requires 5V fixed DC voltage, so 7805 regulator IC rated for 1A of output current is selected.

Selection of Bypass Capacitors:

The data sheet on the 7805 series of regulators states that for best stability, the input bypass capacitorshould be 0.33µF. The input bypass capacitor is needed even if the filter capacitor is used. The large electrolytic capacitor will have high internal inductance and will not function as a high frequency bypass; therefore, a small capacitor with good high frequency response is required.

The output bypass capacitor improves the transient response of the regulator and the data sheet recommends a value of 0.1µF.

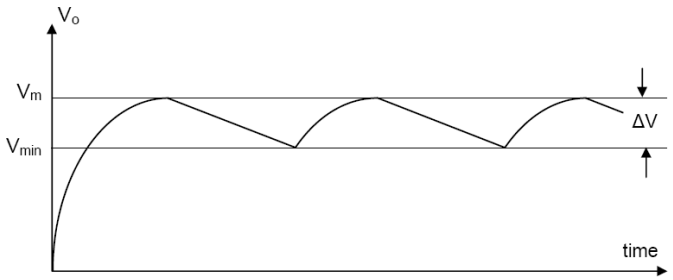
Dropout voltage

The dropout voltage for any regulator states the minimum allowable difference between output and input voltages if the output is to be maintained at the correct level. For 7805, the dropout voltage at the input of theregulator IC is Vo +2.5 V.

$$V_{dropout} = 5+2.5 = 7.5V$$

Selection of Filter Capacitor:

The filter section should have a voltage of at least 7.5V as input to regulator IC.



That is V_{dc} = 7.5 V

Figure 1: Output wave shape from a full-wave filtered rectifier

Ripple voltage = ΔV = Vr

Two figures of merit for power supplies are the ripple voltage, Vr, and the ripple factor,

RF.RF = $V_{r(rms)}$ / V_{dc}

$$V_r(rms) = \frac{V_m - V_{\min}}{2\sqrt{3}} = \frac{V_r}{2\sqrt{3}}$$

$V_{dc} = 2V_m/\pi = 0.636\ V_m$

$$V_{dc} = V_m - \frac{V_r}{2} = \frac{V_m + V_{\min}}{2}$$

Vr = I_L x T_{off}/C can be solved for the value of C.

The ripple frequency of the full-wave ripple is 100 Hz. The off-time of the diodes for 100 Hz ripple is assumedto be 85%. T_{off} = 8.5mS.

C = I_L x T_{off} / Vr =

Selection of Diodes:

1N4007 diodes are used as it is capable of withstanding a higher reverse voltage, PIV of 1000V whereas 1N4001 has PIV of 50V.

Selection of Transformer:

Maximum unregulated voltage, $V_{unreg(max)} = V_{dropout} + Vr$ =

Two diodes conduct in the full-wave bridge rectifier, therefore peak of the secondary voltage must be twodiode drops higher than the peak of the unregulated DC.

$V_{sec(peak)} = V_{unreg\ (max)} + 1.4V = V_{sec(rms)} = 0.707$

$x\ V_{sec(peak)} =$

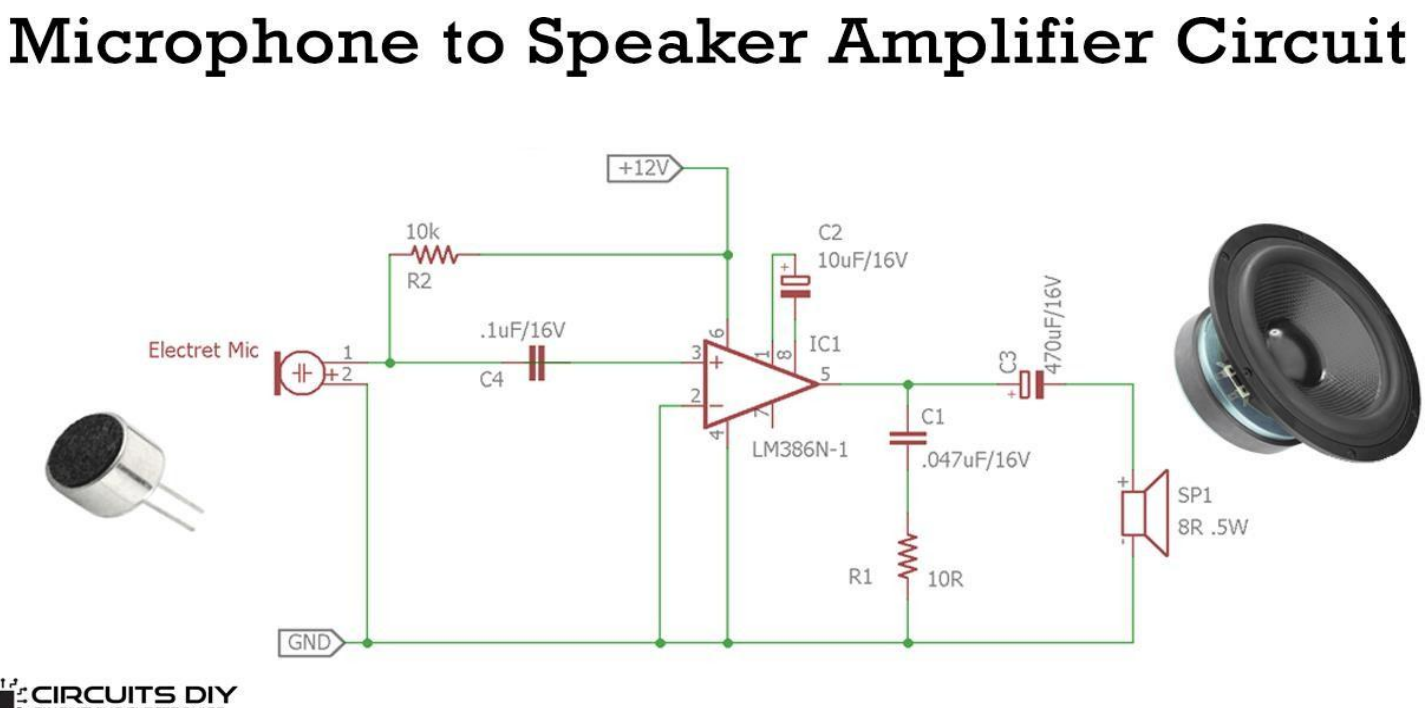
The power supply is designed to deliver 1A of load current, so the secondary winding of the transformer needs to be rated for 1A.

Result:

Experiment No. 12 **Date**:

Design and test an audio amplifier by connecting a microphone input and observe the output using a loudspeaker.

Circuit Diagram:

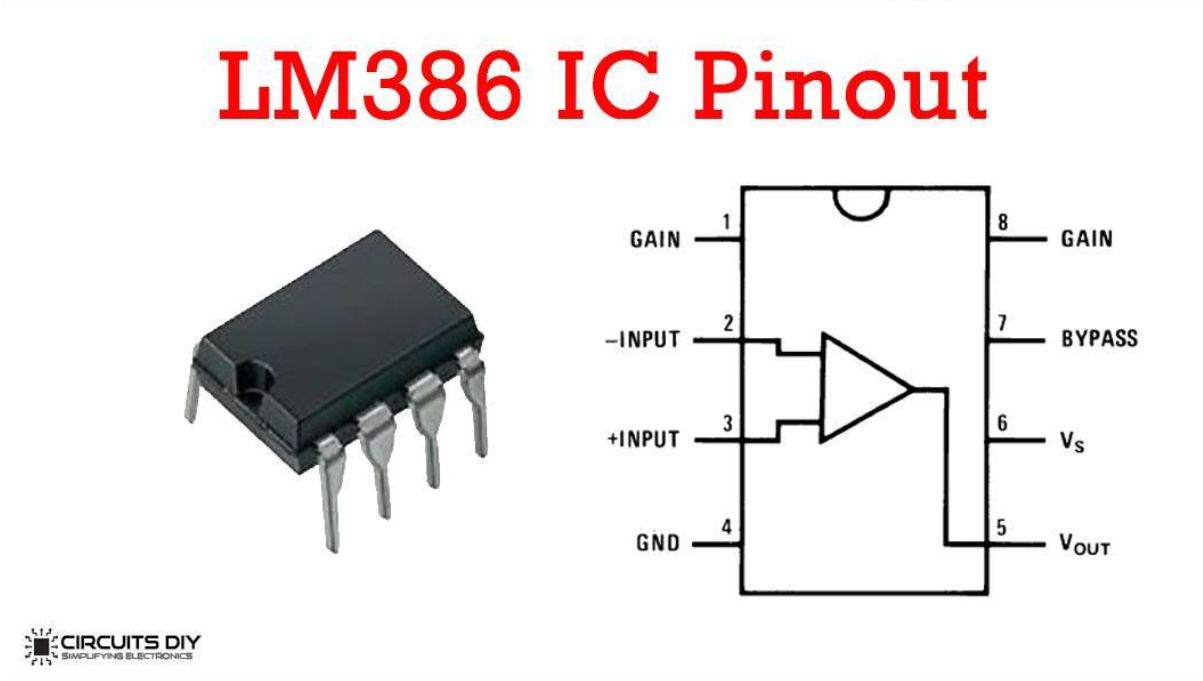


Hardware Components:

The following components are required to make Speaker Amplifier Circuit

S.NO	Component	Value	Qty
1.	Breadboard	–	1
2.	Audio Amplifier IC	LM386	1
3.	Electrolytic Capacitor	10uF, 470uF	1,1

S.NO	Component	Value	Qty
4.	Resistor	10R, 10K	1, 1
5.	Speaker	8 ohms	1
6.	Ceramic Capacitor	0.1uF, 0.047uF	1, 1
7.	Condenser Mic	–	1



Procedure:

(1) Connections are made as shown in the circuit diagram.
(2) Connect the components on the breadboard.
(3) Connect LM386 is an Audio Amplifier IC with respect to pin nos.
(4) Give an audio input signal to the Mic and observe the output in the loudspeaker**.**

Result:

Question Bank for Analog and Digital System Design Laboratory

1. Design and set up the BJT common emitter voltage amplifier without feedback and determine the gain- bandwidth product, input and output impedances.
2. Design and set up the BJT common emitter voltage amplifier with feedback and determine the gain- bandwidth product, input and output impedances.
3. Design and set-up BJT Colpitts Oscillator.
4. Design and set-up BJT Crystal Oscillator.
5. Design Adder circuit using Op-Amp.
6. Design an Integrator circuit using Op-Amp.
7. Design a Differentiator circuit using Op-Amp.
8. Design a Comparator circuit using Op-Amp
9. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
10. Design and implement
    a. Half Adder & Full Adder using basic gates and NAND gates,
    b. Half subtractor & Full subtractor using NAND gates,
    c. 4-variable function using IC74151 (8:1MUX).

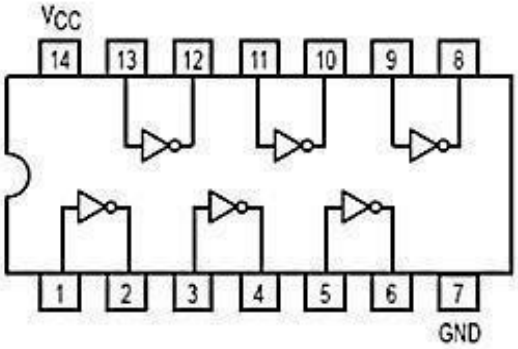
11. Realize
    d. Binary to Gray code conversion & vice-versa (IC74139),
    e. BCD to Excess-3 code conversion and vice versa

12. Realize using NAND Gates:
    f. Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop
        i. Realize the shift registers using IC7474/7495:
    g. (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson counter.

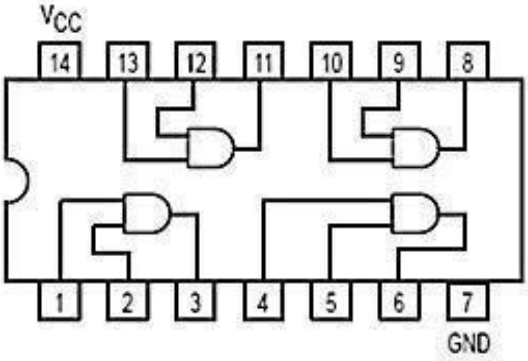
13. Realize
    i. Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop
    ii. Mod-N Counter using IC7490 / 7476
    iii. Synchronous counter using IC74192

IC PIN DETAILS FOR DIGITAL CIRCUITS:

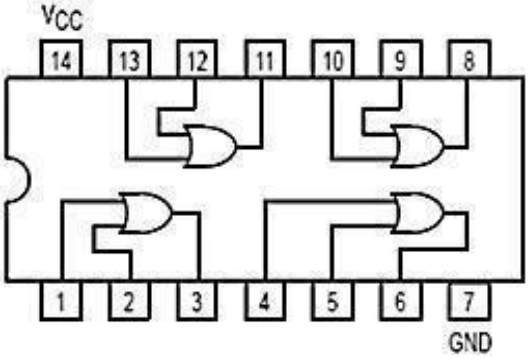
Inverter (NOT Gate) - 7404LS



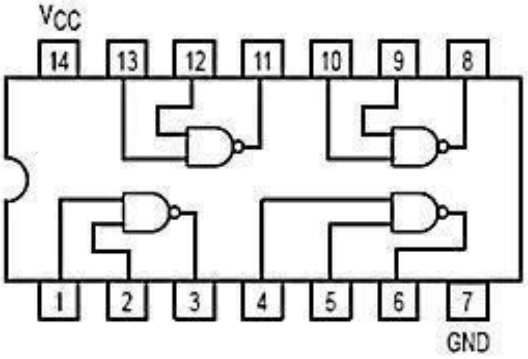
2-Input AND Gate - 7408LS



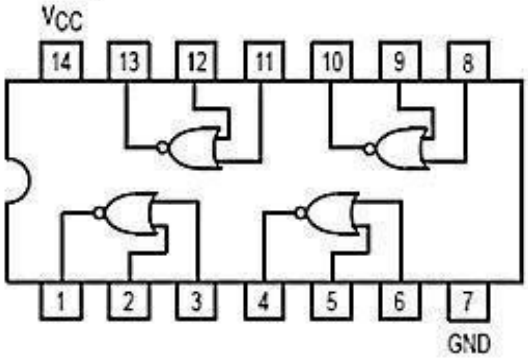
2-Input OR Gate - 7432LS



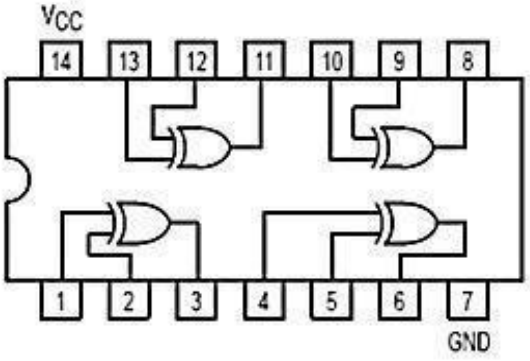
2-Input NAND Gate - 7400LS



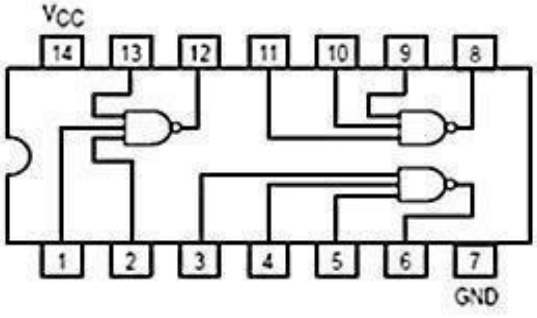
2-Input NOR Gate - 7402LS



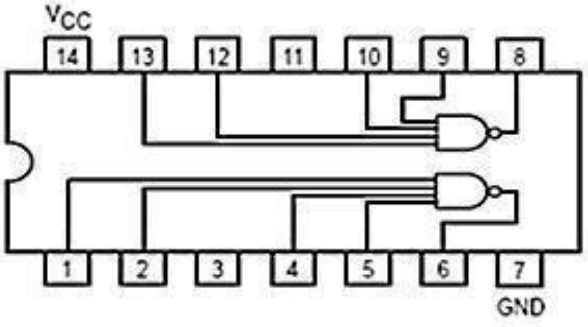
2-Input EX-OR Gate - 7486LS

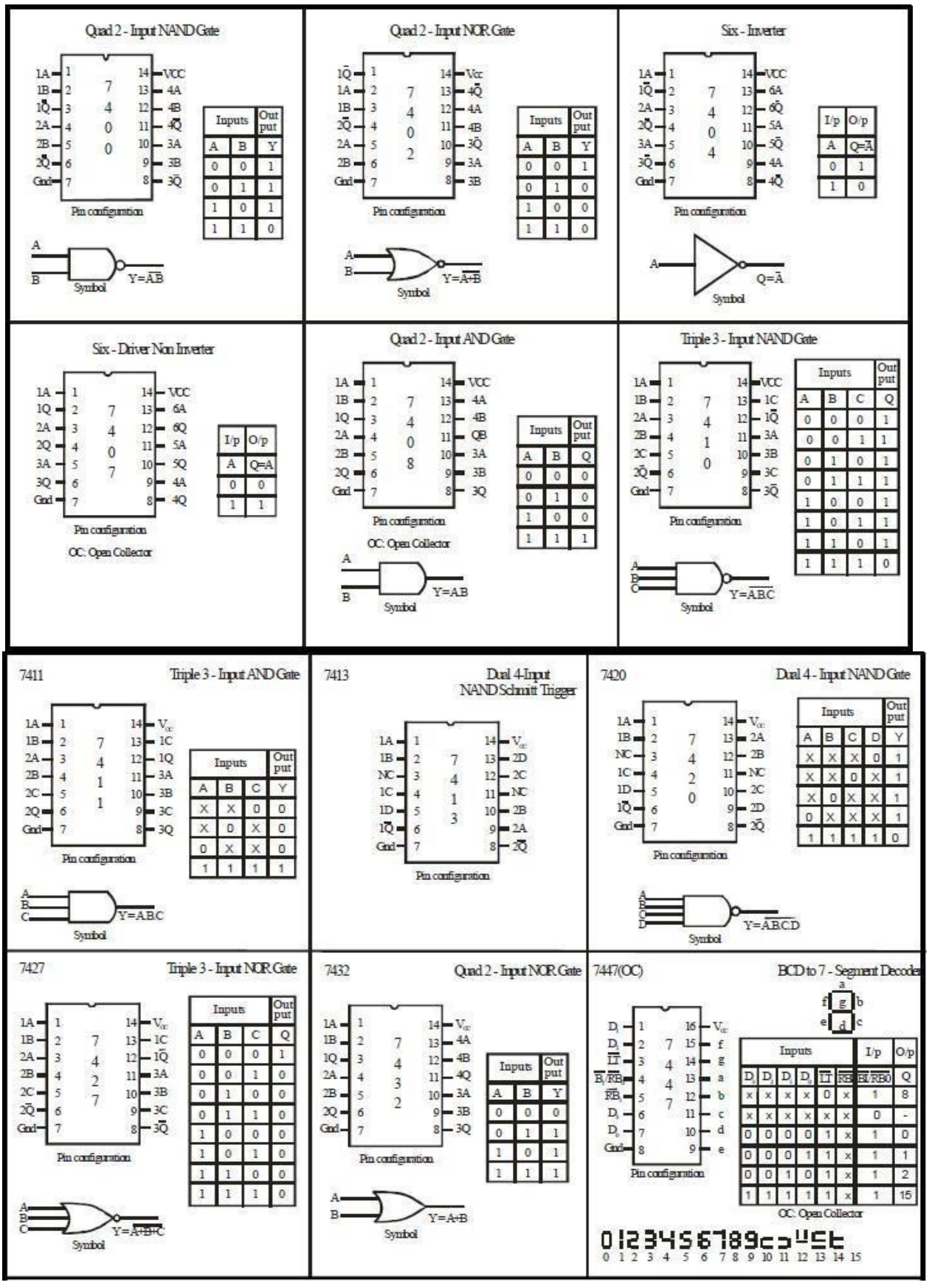


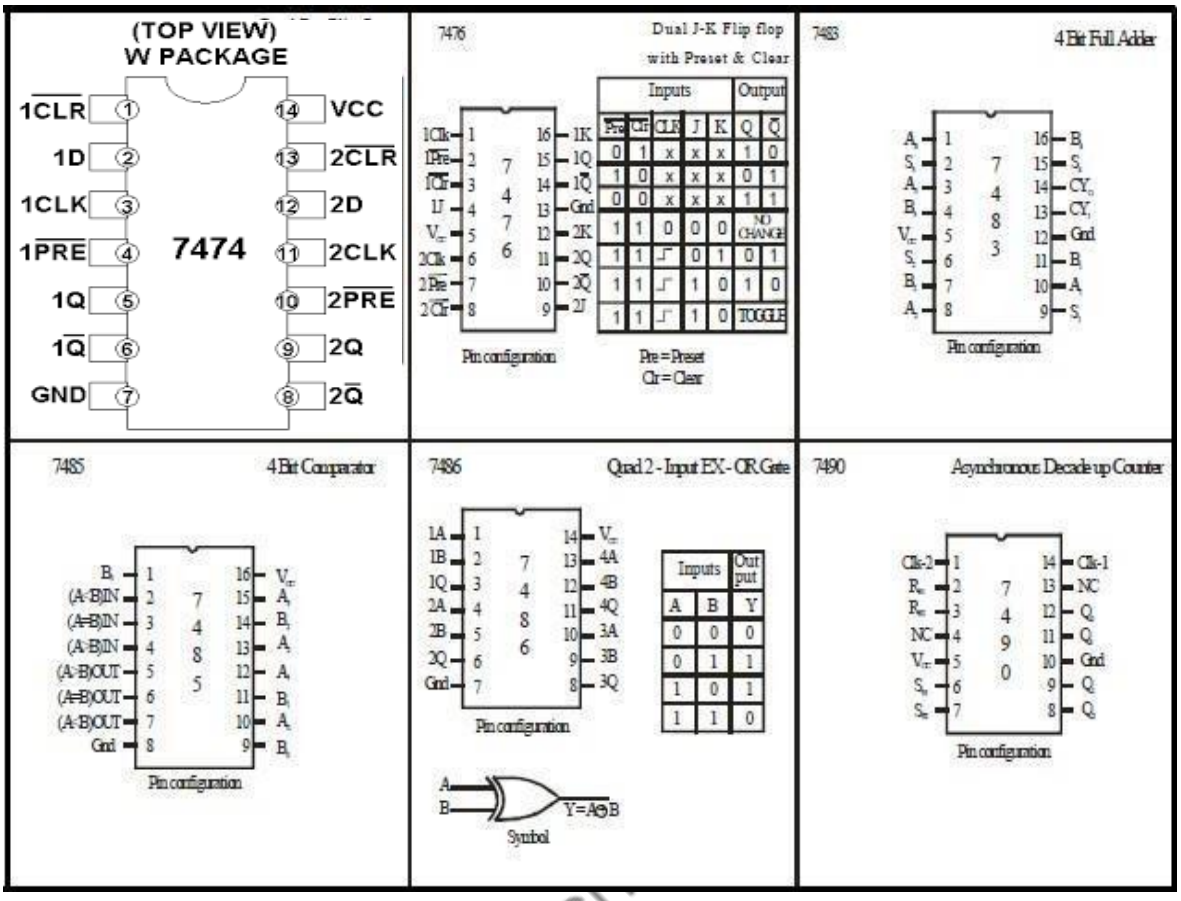
3-Input NAND Gate - 7410LS

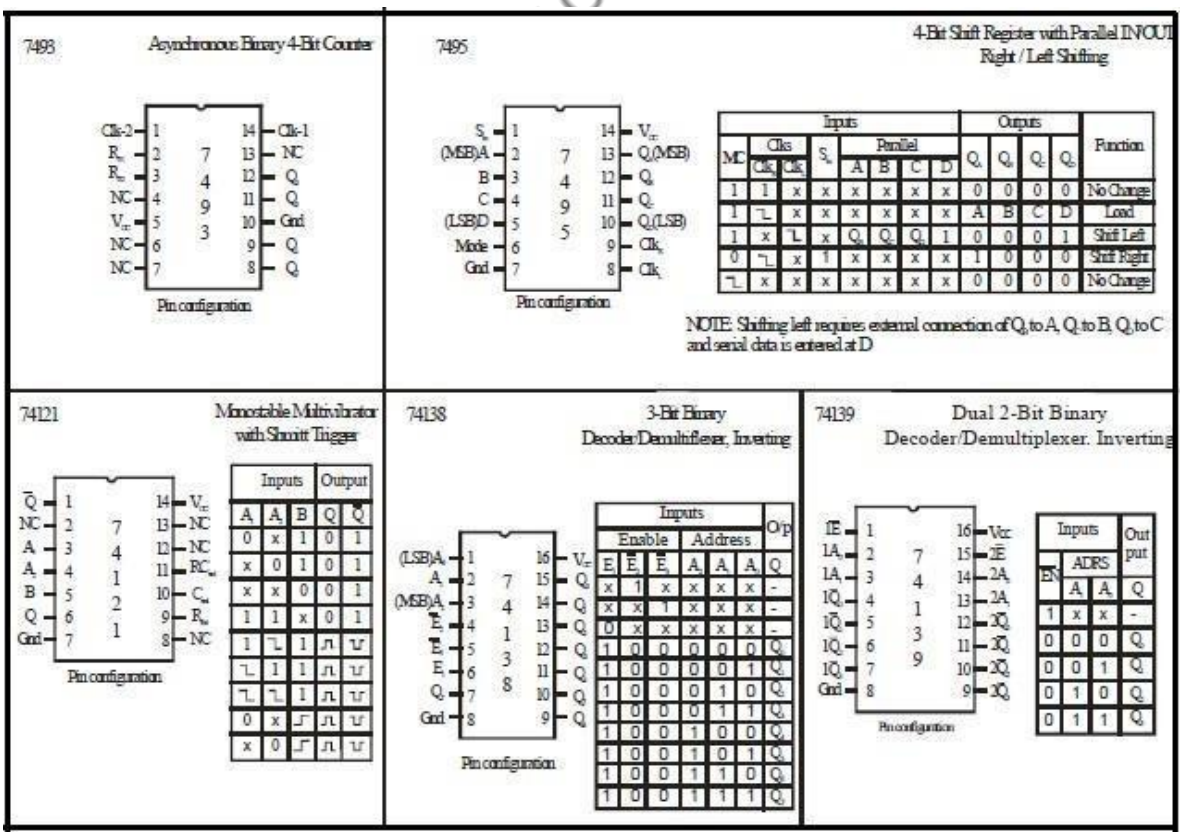


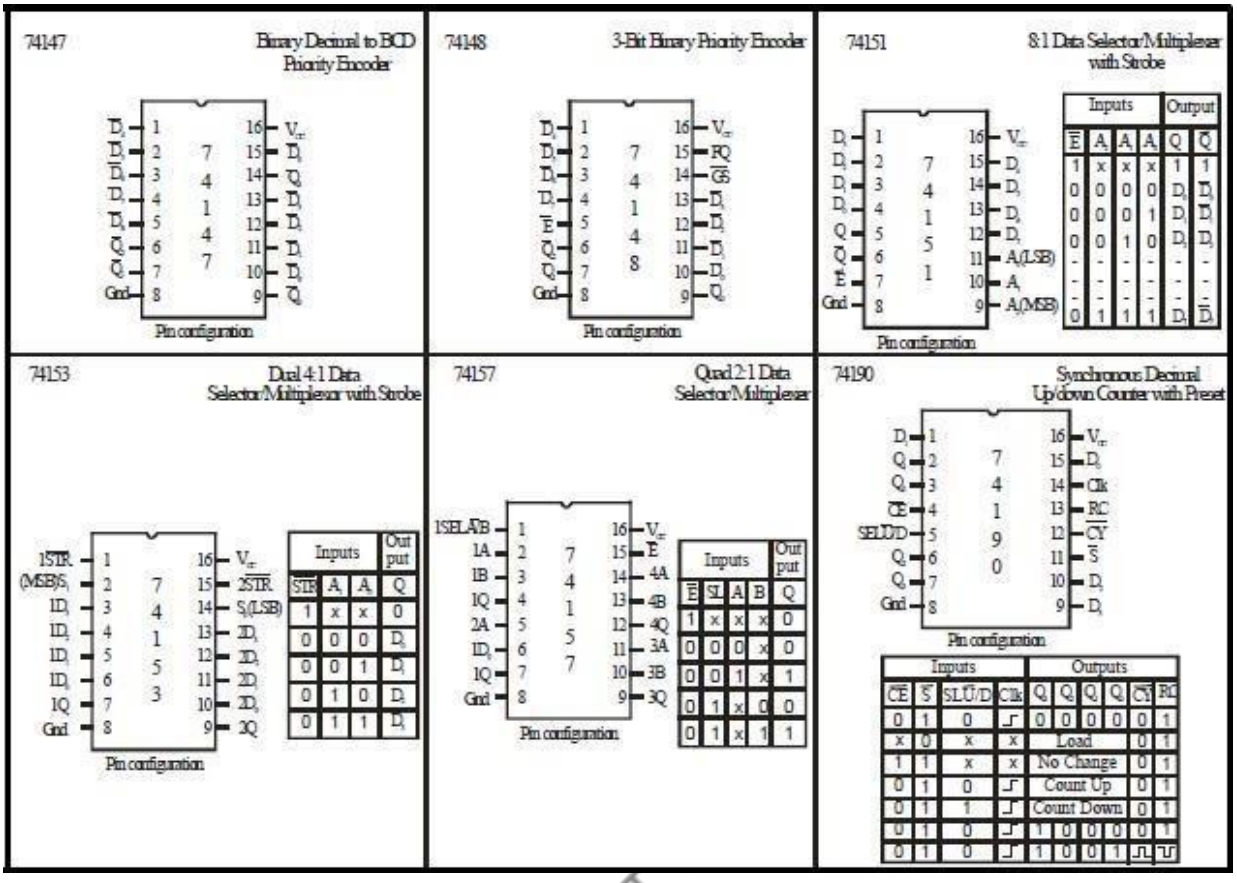
Dual 4-Input NAND Gate - 7420LS

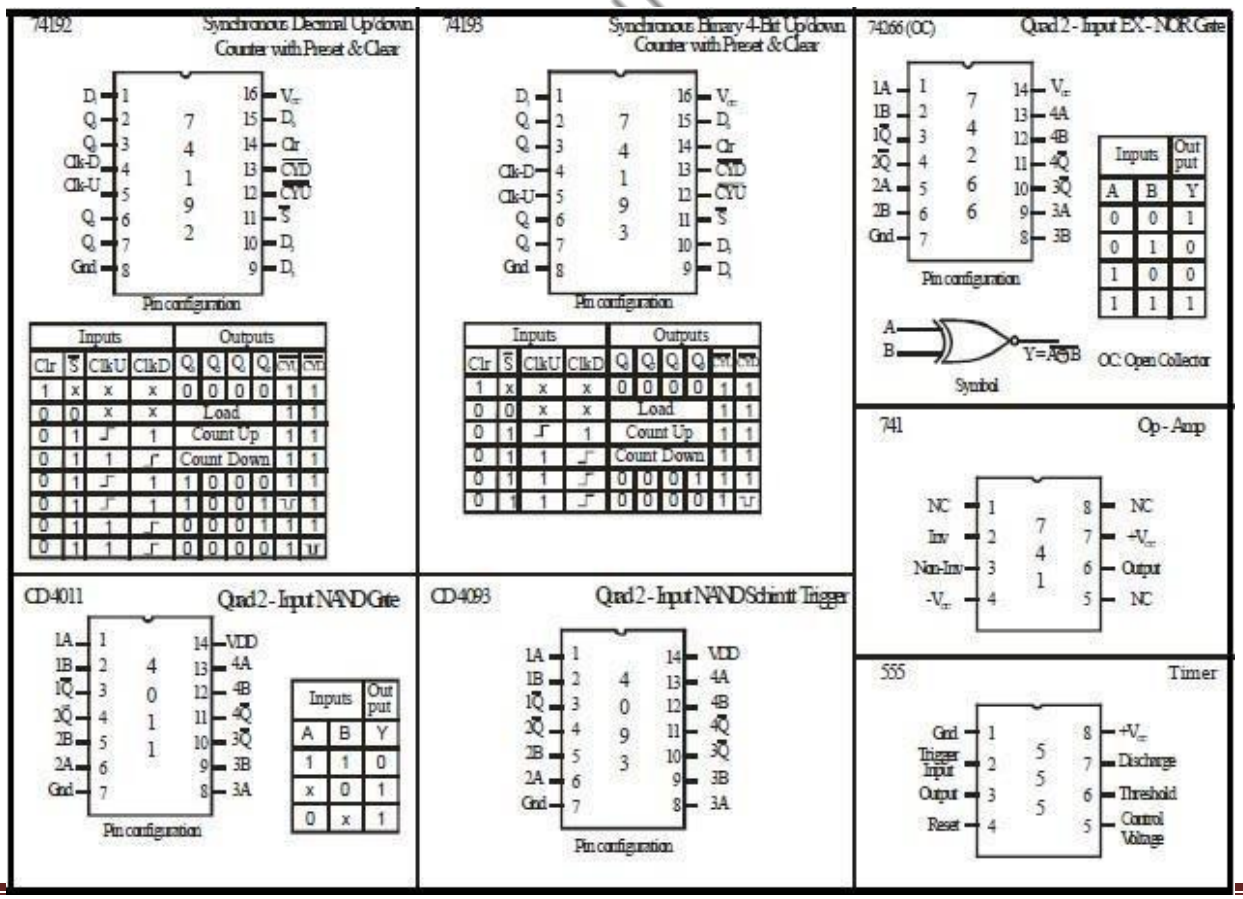



Quad 2 - Input NAND Gate
Pin configuration
Symbol
Y=$\overline{AB}$
Quad 2 - Input NOR Gate
Pin configuration
Symbol
Y=$\overline{A+B}$
Six - Inverter
Pin configuration
Symbol
Q=$\bar{A}$
Six - Driver Non Inverter
Pin configuration
OC: Open Collector
Quad 2 - Input AND Gate
Pin configuration
OC: Open Collector
Symbol
Y=AB
Triple 3 - Input NAND Gate
Pin configuration
Symbol
Y=$\overline{ABC}$
7411
Triple 3 - Input AND Gate
Pin configuration
Symbol
Y=ABC
7413
Dual 4-Input NAND Schmitt Trigger
Pin configuration
7420
Dual 4 - Input NAND Gate
Pin configuration
Symbol
Y=$\overline{ABCD}$
7427
Triple 3 - Input NOR Gate
Pin configuration
Symbol
Y=$\overline{A+B+C}$
7432
Quad 2 - Input NOR Gate
Pin configuration
Symbol
Y=A+B
7447(OC)
BCD to 7 - Segment Decoder
Pin configuration
OC: Open Collector

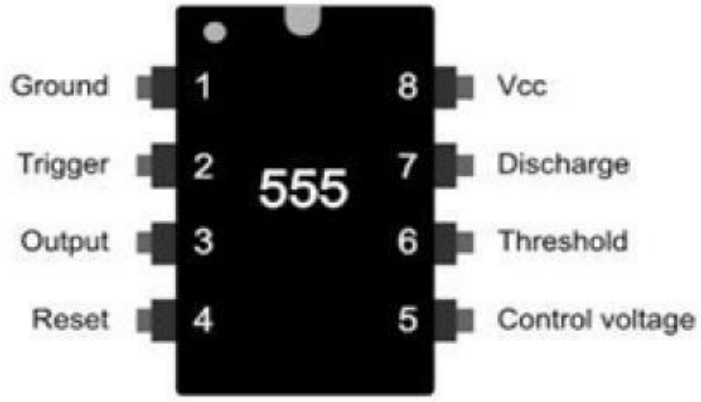

(TOP VIEW)
W PACKAGE
1CLR
1D
1CLK
1PRE
1Q
1Q
GND
VCC
2CLR
2D
2CLK
2PRE
2Q
2Q
7474
7476
Dual J-K Flip flop with Preset & Clear
Pin configuration
Pre=Preset
Clr=Clear
7483
4 Bit Full Adder
Pin configuration
7485
4 Bit Comparator
Pin configuration
7486
Quad 2 - Input EX - OR Gate
Pin configuration
Symbol
7490
Asynchronous Decade up Counter
Pin configuration


7493
Asynchronous Binary 4-Bit Counter
Pin configuration
7495
4-Bit Shift Register with Parallel IN/OUT Right / Left Shifting
Pin configuration
NOTE: Shifting left requires external connection of Q to A, Q to B, Q to C and serial data is entered at D
74121
Monostable Multivibrator with Shmitt Trigger
Pin configuration
74138
3-Bit Binary Decoder/Demultiplexer, Inverting
Pin configuration
74139
Dual 2-Bit Binary Decoder/Demultiplexer. Inverting
Pin configuration

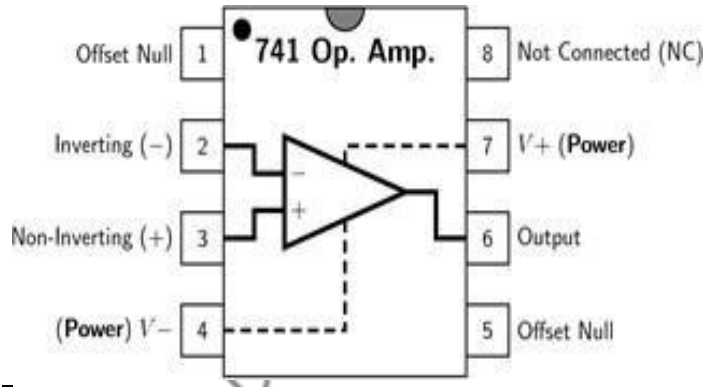

74147
Binary Decimal to BCD Priority Encoder
74148
3-Bit Binary Priority Encoder
74151
8:1 Data Selector/Multiplexer with Strobe
74153
Dual 4:1 Data Selector/Multiplexer with Strobe
74157
Quad 2:1 Data Selector/Multiplexer
74190
Synchronous Decimal Up/down Counter with Preset
Pin configuration


74192
Synchronous Decimal Up/down Counter with Preset & Clear
74193
Synchronous Binary 4-Bit Up/down Counter with Preset & Clear
74266 (OC)
Quad 2 - Input EX - NOR Gate
OC: Open Collector
Symbol
741
Op - Amp
555
Timer
CD4011
Quad 2 - Input NAND Gate
CD4093
Quad 2 - Input NAND Schmitt Trigger
Pin configuration

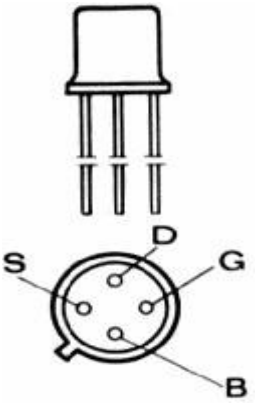
PIN CONFIGURATIONS FOR ANALOG CIRCUITS



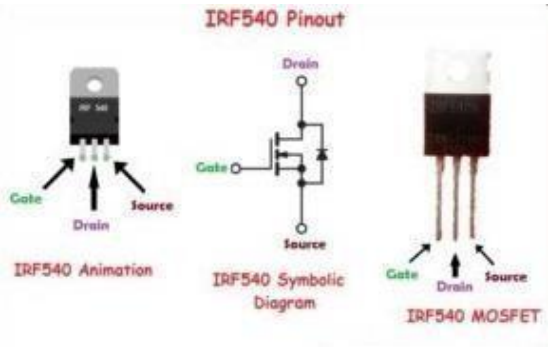
555 timer pin diagram



Op-Amp µA741 pin diagram



JFET BFW10Pinout



MOSFET IRF540N Pinout

Additional Experiments OR Beyond the Syllabus

Experiment No.1 **Date:**

Frequency Modulation Using IC 8038/2206 and Demodulation

Aim: To generate Frequency Modulated wave and to demodulate it. Also find frequency deviation and modulation index.

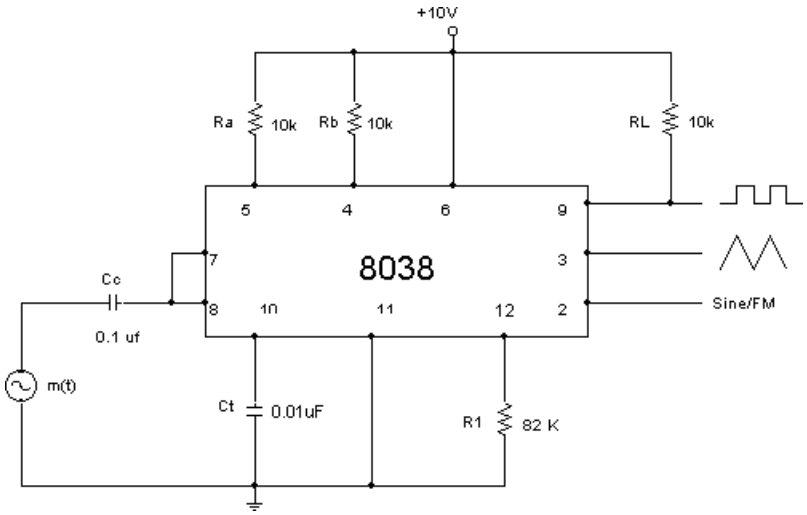
Apparatus Required:

Sl.No.	Particulars	Range	Quantity
1.	IC 8038, IC 565	-	1
2.	Resistors & Capacitors	As per design	1 each
3.	CRO Probes	-	2 set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram.
3. By switching off the modulating signal m(t) note the frequency of the carrier wave
   at Pin No.2 of IC-8038.
4. Apply the modulating signal with suitable amplitude to get the FM signal.
5. Note the maximum (f_{cmax}) and minimum (f_{cmin}) frequency of the carrier wave in FM signal.
6. Calculate the frequency deviation, modulation index and bandwidth.
7. Feed the FM wave to the demodulator circuit and observe the output.
8. Note down frequency and amplitude of the demodulated output waveform.

Circuit Diagram: FM Modulation



Design:

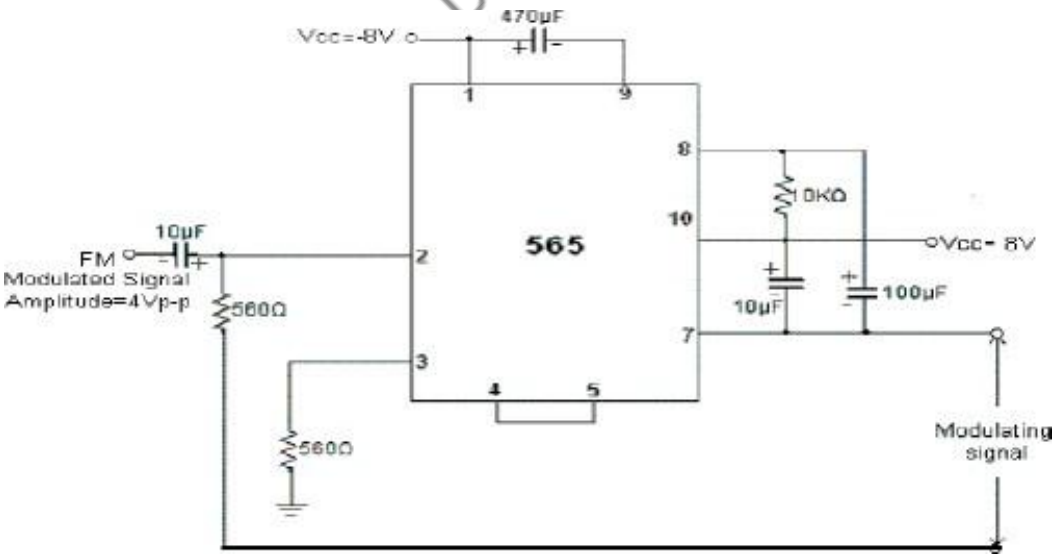
Specifications: Carrier frequency f_c = 3 kHz

$f_c = 0.3 / (R C_t)$ Where $R = R_a = R_b$

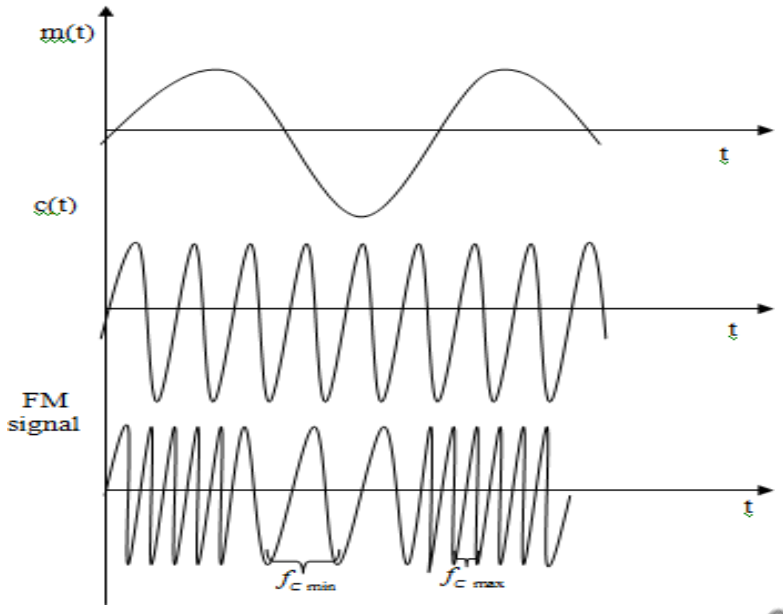
Assume $R = R_a = R_b = 10\ k\Omega$ then $C_t = 0.01\ \mu F$

Choose RL = 10 kΩ, R1 = 82 kΩ, Cc= 0.1 μF

Circuit Diagram: Demodulation:



Waveforms:



Demodulated signal

Tabular Column:

fc = _____Hz, fm = _____Hz

Where $\partial_1 = f_{C\,max} - f_C$, $\partial_2 = f_C - f_{C\,min}$

Sl. No.	**V_m in V**	**$f_{c\,max}$ In Hz**	**$f_{c\,min}$ In Hz**	**δ_1 in Hz**	**δ_2 in Hz**	**δ in Hz**	**$\beta = \delta/fm$**	**$B_T = 2\delta + 2fm$ In Hz**

Result:

Modulation index = _____

Maximum Frequency Deviation = ___Hz.

Bandwidth of Operation = _____Hz.

Demodulated frequency=_____Hz.

Experiment No.2 **Date:**

TIME DIVISION MULTIPLEXING

Aim: To study Time Division Multiplexing for 2 band-limited signals.

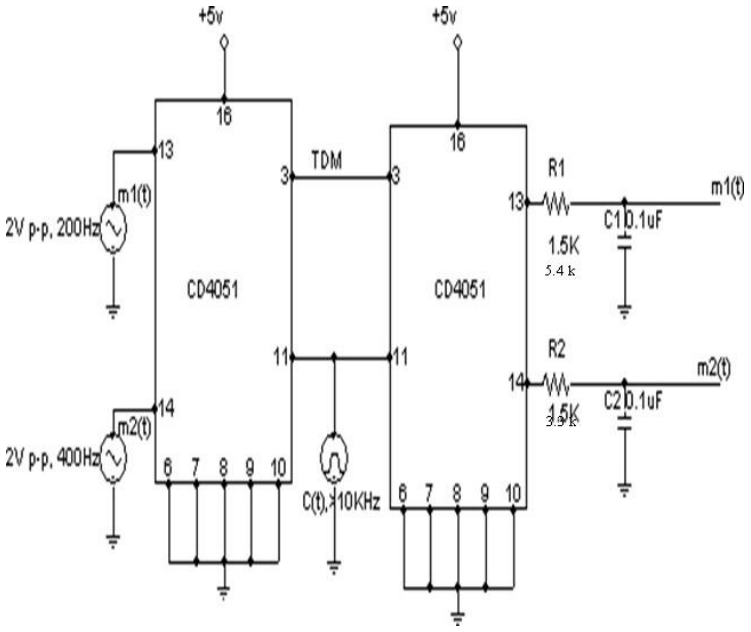
Apparatus Required:

Sl No	Apparatus	Range	Quantity
1	IC CD 4051		2
2	Resistors	As Per Design	2
3	Capacitor	As Per Design	2

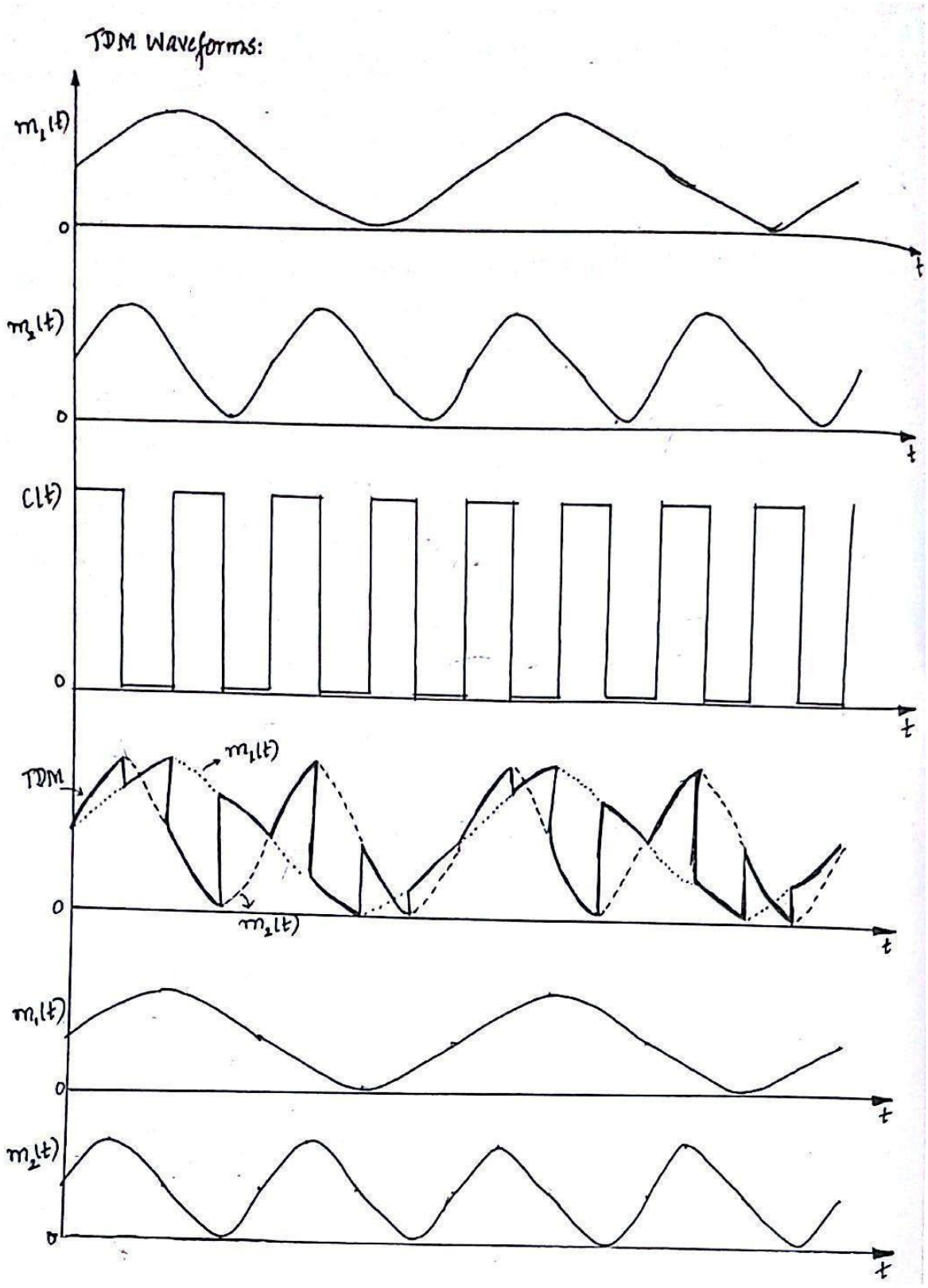
Procedure:

1. Connections are made as shown in the circuit diagram.
2. Apply a square wave (TTL) carrier signal of 2 kHz (or >2 kHz) of 5Vamplitude.
3. Apply $m_1(t)$ and $m_2(t)$ whose frequencies are f_1 (200 Hz, with DC offset) and f_2 (400 Hz, with DC offset).
4. Observe TDM waveform at pin number 3 of ICCD4051.
5. Observe the reconstructed message waveforms $m_1(t)$ and $m_2(t)$ at pin numbers 13 and 14 of 2nd ICCD4051.
6. The ripples in the demodulated signals can be reduced by increasing the order of the filter or by increasing the carrier frequency.

Circuit diagram: TDM of 2 band-limited signals



TDM Waveforms:



Design:

Low pass filter:

a) For messagesignal-1

$f_c = 1/(2\pi RC)$

Let

$f_c = 300$ Hz, C1 =0.1µF.

$R1 = 1/(2\pi x300x0.1x10^{-6})$

$R1 = 5.305\ K\Omega \approx 5.4\ K\Omega$

b) For messagesignal-2

$f_c = 1/(2\pi RC)$

Let

f_c=500z, and C2=0.1µF.

$R2=1/(2\pi x500x0.1x10^{-6})$

$R2 = 3.183\ K\Omega \approx 3.3K\Omega$

Result: