QMP 7.1 D/F

Channabasaveshwara Institute of Technology
(Affiliated to VTU, Belgaum & Approved by AICTE, New Delhi)
(**NAAC Accredited & ISO 9001:2015 Certified Institution)**
NH 206 (B.H. Road), Gubbi, Tumkur – 572 216. Karnataka

Department of Electronics & Communication Engineering

ANALOG CIRCUITS LABORATORY

18ECL48

B.E - IV Semester

Lab Manual 2019-20

Name : _____

USN : _____

Batch :_____Section : _____

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Department of Electronics & Communication Engineering

Analog Circuits Laboratory

Version 4.0

February 2020

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INSTITUTE VISION

To create centres of excellence in education and to serve the society by enhancing the quality of life through value based professional leadership.

INSTITUTE MISSION

- To provide high quality technical and professionally relevant education in a diverse learning environment.
- To provide the values that prepare students to lead their lives with personal integrity, professional ethics and civic responsibility in a global society.
- To prepare the next generation of skilled professionals to successfully compete in the diverse global market.
- To promote a campus environment that welcomes and honors women and men of all races, creeds and cultures, values and intellectual curiosity, pursuit of knowledge and academic integrity and freedom.
- To offer a wide variety of off-campus education and training programmes to individuals and groups.
- To stimulate collaborative efforts with industry, universities, government and professional societies.
- To facilitate public understanding of technical issues and achieve excellence in the operations of the institute.

QUALITY POLICY

Our organization delights customers (students, parents and society) by providing value added quality education to meet the national and international requirements. We also provide necessary steps to train the students for placement and continue to improve our methods of education to the students through effective quality management system, quality policy and quality objectives.

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Vision

To create globally competent Electronics and Communication Engineering professionals with ethical and moral values for the betterment of the society

Mission

- To nurture the technical/professional/engineering and entrepreneurial skills for overall self and societal upliftment through co-curricular and extra-curricular events.
- To orient the Faculty/Student community towards the higher education, research and development activities.
- To create the Centres of Excellence in the field of electronics and communication in collaboration with industries/Universities by training the faculty through latest technologies.
- To impart quality technical education in the field of electronics and communication engineering to meet over the current/future global industry requirements.

Program Educational Objectives (PEO's)

After four Years of Graduation, our graduates are able to:

- Provide technical solutions to real world problems in the areas of electronics and communication by developing suitable systems.
- Pursue engineering career in Industry and/or pursue higher education and research.
- Acquire and follow best professional and ethical practices in Industry and Society.
- Communicate effectively and have the ability to work in team and to lead the team.

Program Specific Outcomes (PSO's)

At the time of graduation, our graduates are able to:

- **PSO1**: Build Analog and Digital Electronic systems for Multimedia Applications, VLSI and Embedded Systems in Interdisciplinary Research / Development.
- **PSO2**: Design and Develop Communication Systems as per Real Time Applications and Current Trends.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

SYLLABUS

B. E. (EC / TC) Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – IV			
ANALOG CIRCUITS LABORATORY			
Laboratory Code	**18ECL48**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**
CREDITS – 02			
Laboratory Experiments			
PART A : Hardware Experiments			
1. Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.			
2. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.			
3. Design and set-up BJT/FET i) Colpitts Oscillator, and ii) Crystal Oscillator			
4. Design active second order Butterworth low pass and high pass filters.			
5. Design Adder, Integrator and Differentiator circuits using Op-Amp			
6. Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.			
7. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.			
8. Design Monostable and a stable Multivibrator using 555 Timer.			
PART-B : Simulation using EDA software (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any other equivalent tool can be used)			
1. RC Phase shift oscillator and Hartley oscillator			
2. Narrow Band-pass Filter and Narrow band-reject filter			
3. Precision Half and full wave rectifier			
4. Monostable and A stable Multivibrator using 555 Timer.			
Conduct of Practical Examination: • All laboratory experiments are to be included for practical examination. • Students are allowed to pick one experiment from the lot. • Strictly follow the instructions as printed on the cover page of answer script for breakup of marks. • Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.			

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Department of Electronics and Communication Engineering

Analog Circuit Laboratory: Course Objectives and Outcomes

COURSE OBJECTIVES :

The main objectives of this lab are,

- To create environment to understand the operation of analog modulation techniques and Linear IC Applications.
- To design and understand the importance of op-amp (uA 741) in various applications like Low Pass & High Pass Filters, DAC, adder, differentiator, integrator and Oscillator Circuits.
- To study and design the application of 555 timer like astable and monostable multivibrator.
- Use of circuit simulation for the analysis of electronic circuits.
- Understand the circuit configuration and connectivity of BJT and FET Amplifiers and study of frequency response

COURSE OUTCOMES :

After completing this course the student could be able to:

CO1: Design and implement Analog circuits using BJT and FET

CO2: Design Analog circuits using OPAMPs for different applications

CO3: Design of 555 timer for Monostable and astable Multivibrator

CO4: Simulate and analyze Analog circuits that uses ICs for different electronic applications

CO5: Construct simple applications such as RPS, square wave generator, DAC and dead zone circuit.

'Instructions to the Candidates'

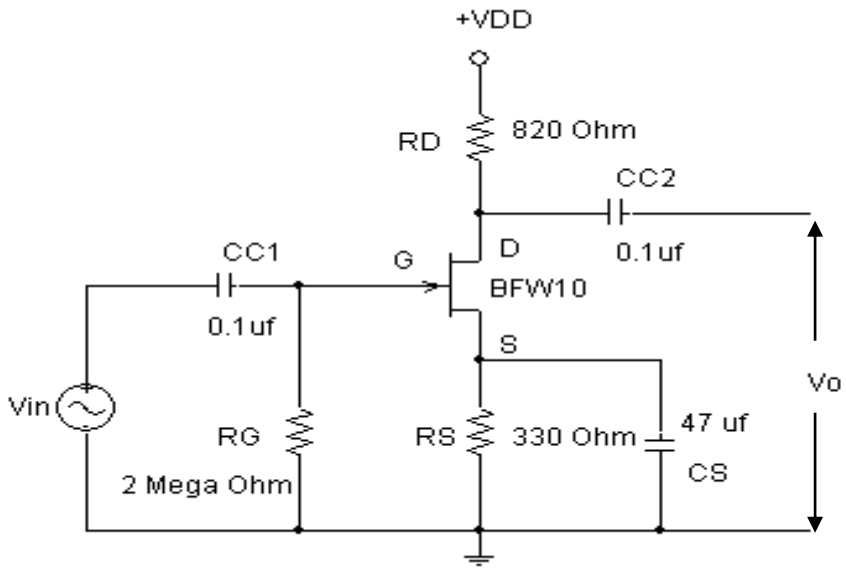
- Student should come with thorough preparation for the experiment to be conducted.
- Student should take prior permission from the concerned faculty before availing the leave.
- Student should come with proper dress code and to be present on time in the laboratory.
- Student will not be permitted to attend the laboratory unless they bring the practical record fully completed in all respects pertaining to the experiment conducted in the previous class.
- Student will not be permitted to attend the laboratory unless they bring the observation book fully completed in all respects pertaining to the experiment to be conducted in present class.
- Experiment should be started conducting only after the staff-in-charge has checked the circuit diagram.
- All the calculations should be made in the observation book. Specimen calculations for one set of readings have to be shown in the practical record.
- Wherever graphs to be drawn, A-4 size graphs only should be used and the same should be firmly attached in the practical record.
- Practical record and observation book should be neatly maintained.
- Student should obtain the signature of the staff-in-charge in the observation book after completing each experiment.
- Theory related to each experiment should be written in the practical record before procedure in your own words with appropriate references.

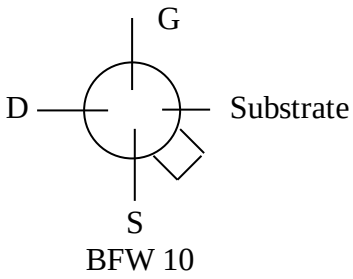
CONTENTS

INDEX PAGE

Sl. No	Name of the Experiment	Date			Manual Marks (Max . 20)	Record Marks (Max. 10)	Signature (Student)	Signature (Faculty)
		Conduction	Repetition	Submission of Record				
1	Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.							
2	Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.							
3	Design and set-up BJT/FET i) Colpitts Oscillator, and ii) Crystal Oscillator							
4	Design active second order Butterworth low pass and high pass filters.							
5	Design Adder, Integrator and Differentiator circuits using Op-Amp							
6	Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.							
7	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.							
8	Design Monostable and a stable Multivibrator using 555 Timer.							
9	Simulation using EDA software for RC Phase shift oscillator and Hartley oscillator							
10	Simulation using EDA software for Narrow Band-pass Filter and Narrow band-reject filter							
11	Simulation using EDA software for Precision Half and full wave rectifier							
12	Simulation using EDA software for Monostable and A stable Multivibrator using 555 Timer.							
Average								

Circuit Diagram : RC Coupled Single Stage FET Amplifier





Design

Given V_{DD} = 10 V, V_{GS}(off) = -4 V I_{DSS} (max) = 12 mA R_G = 2 MΩ

Formulae

$I_D = I_{DSS}.(1 – V_{GS} / V_{GS}(off))^2$ ----------(1)

When V_G = 0, Then $V_S = -V_{GS}$

But $V_S = I_D . R_S$

When V_G = 0, $I_D = I_{DSS}$

$V_S = I_{DSS}.R_S$

$I_{DSS}.R_S = -V_{GS}(off)$

$R_S = -(-4) / 12mA = 333\ \Omega$

Choose $\mathbf{R_S = 330\ \Omega}$

From (1)

$I_D = I_{DSS}.(1 – I_D.R_S / V_{GS}(off))^2$

$I_D = I_{DSS}.(1 + I_D^2.R_S^2 / 16 - I_D.R_S/2)$

$I_D = 12 \times 10^{-3} \times (1 + I_D^2.330^2 / 16 - I_D.330/2)$

$81.675I_D^2 - 2.98I_D + 12 \times 10^{-3} = 0$

I_D = 4.6 mA or I_D = 31.9 mA

Since I_D cannot be greater than I_{DSS}, Choose I_D = 4.6 mA

Assume V_{DS} = 50 % V_{DD} ---- V_{DS} = 5V

Applying KVL to output circuit

$V_{DD} = I_D . R_D + V_{DS} + I_D .R_S$

Experiment No: 1 **Date:**

RC Coupled Single Stage FET Amplifier

Aim: To conduct an experiment to plot the frequency response of an RC coupled amplifier and to find the input impedance, output impedance and the voltage gain.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	FET BFW 10	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory:

An amplifier is a circuit which increases the voltage, current or power level of i/p signal where the frequency is maintained constant from o/p to i/p signal. In FET amplifier the output current (I_D) is a function of input voltage V_{GS}. That is as V_{GS} varies the drain current varies. V_{GS} varies as input signal varies in turn the drain current varies hence amplification takes place. In R_C coupled FET amplifier R_D and R_S are selected in such a way that FET operates in active region and the operating point will be in the middle of active region. Coupling capacitors C_{C1} and C_{C2} are used to block dc current flow through load and the source. The source by-pass capacitor C_S is connected to avoid negative feedback.

An amplifier in which resistance-capacitance coupling is employed between stages and at the input and output point of the circuit is known as RC coupled amplifier. A capacitor provides a path for signal currents between stages, with resistors connected from each side of the capacitor to the power supply or to ground.

Procedure:

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram.
3. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
4. By disconnecting the AC source measure the quiescent point (V_{DS} and $I_D = V_{RD} / R_D$)

Applications:

1. FET amplifiers are low noise amplifiers used for front-end applications.
2. They are used in Oscillators.
3. These are faster and are less noisy compared to BJT amplifiers.

$R_D = (10 – 5 – 4.6 \times 10^{-3} \times 330) / 4.6 \times 10^{-3}$

$R_D = 756\ \Omega$

Choose $\mathbf{R_D = 820\ \Omega}$

$X_{CS} << R_S$

$X_{CS} = R_S / 10$

$1 / (2 \pi f C_S) = 470 / 10$ Let f = 100 Hz

$C_S = 33\ \mu F$ Choose $\mathbf{C_S = 47\ \mu F}$

Choose $C_{C1} = C_{C2} = 0.1\ \mu F$

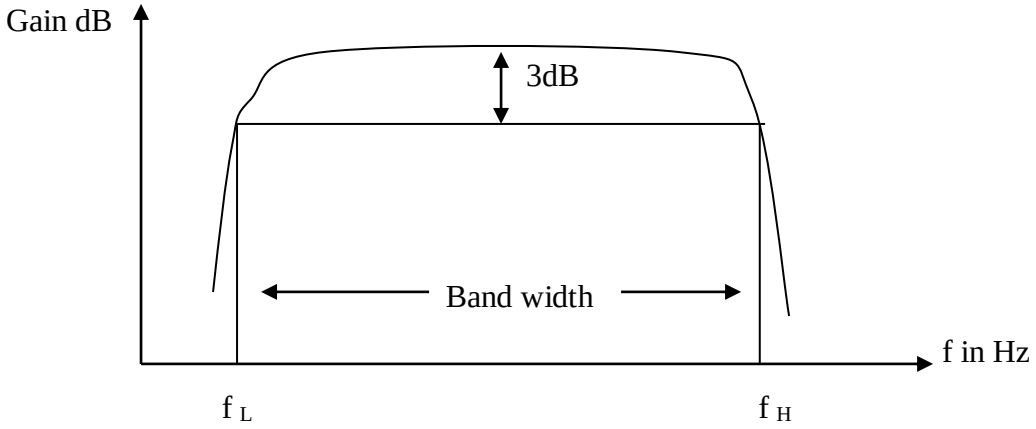
Tabular Column : V_i = _____ V

f in Hz	**V_o in Volt**	**$A_V = V_o / V_i$**	**Gain in dB = 20*log A_V**

To find frequency response:

1. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
2. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
3. Calculate AV and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and band width.
4. Calculate figure of merit.

Ideal Graph

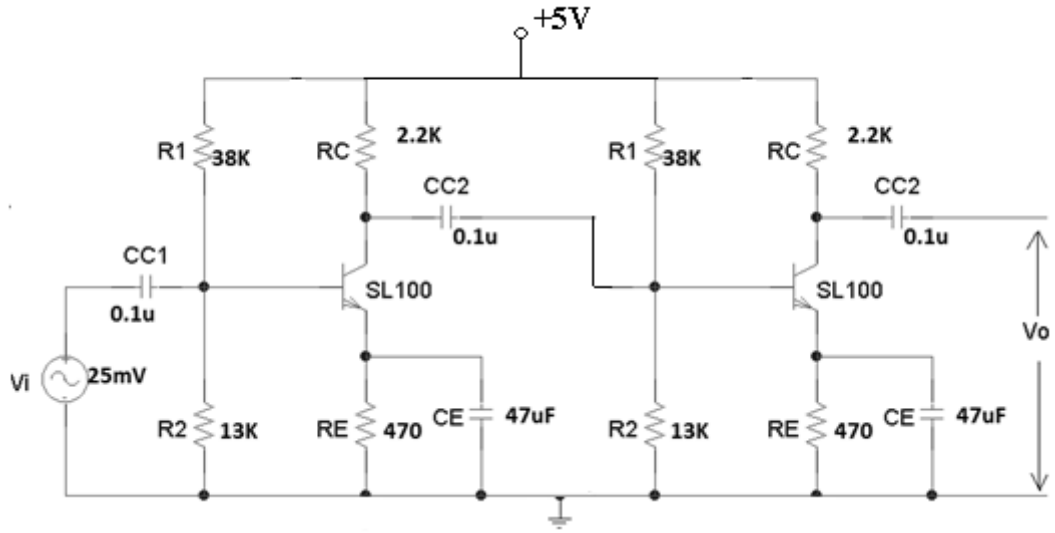


f_L = Lower cutoff frequency f_H = Higher cutoff frequency

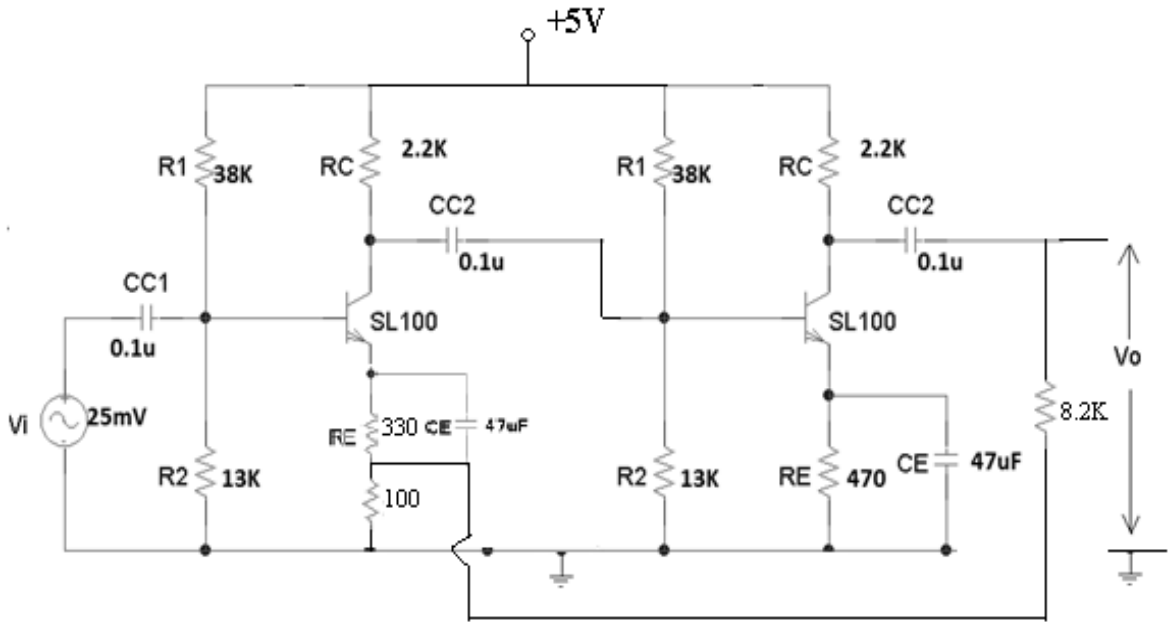
Result:

1. Quiescent point : V_{DS} = ____ V, I_D = _____ mA, V_{GS} = _____ V
2. Voltage Gain (A_V) = _____ (in mid band region)
3. Bandwidth (BW) = _____ Hz
4. Figure of merit (FM = A_V * BW) = _____ Hz

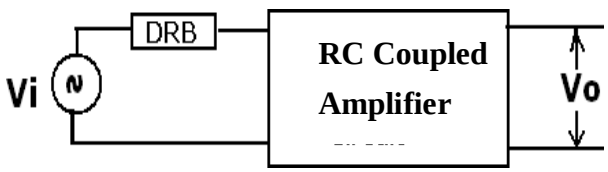
Circuit Diagram : Without feedback



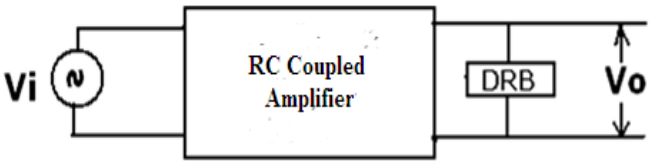
Circuit Diagram : With feedback



To measure Z_i :



To measure Z_0 :



Experiment No :2 **Date:**

Two Stage Voltage Series Feedback Amplifier

Aim: To conduct an experiment to plot the frequency response of an two stage amplifier with and without feedback and to find the input impedance, output impedance and the voltage gain.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	BJT	-	02
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DRB	-	01
6.	Spring board and connecting wires	-	-

Theory:

Feedback is the process of combining a portion of output signal with input signal. There are two types of feedback namely positive feedback and negative feedback. If the signal fed back is in phase with the input signal we call it as positive feedback and if the fed back signal is out of phase with the input signal we call it as negative feedback.

Positive feedback is used in oscillators to develop oscillations, where as negative feedback is used in amplifiers to improve the characteristics of amplifiers. There are four types of feedback concepts name voltage series feedback, current series feedback, voltage shunt feedback and current shunt feedback. In this experiment we discuss voltage series feedback. In voltage series feedback the input impedance will increase, output impedance will decrease, bandwidth increases and distortion decreases which are all advantages but the voltage gain decreases which is a disadvantage which can be improved by cascading with other amplifier.

Procedure: (Without Feedback)

1. Components / Equipment are tested for their good working condition.
2. Connections are made as shown in the circuit diagram.
3. By keeping the voltage knobs in minimum position and current knob in maximum position switch on the power supply.
4. By disconnecting the AC source measure the quiescent point (V_{CE} and I_C)

Design:

Given, $\mathbf{V_{CE} = 2.5\ V}$ and $\mathbf{I_C = 1\ mA}$ Assume $\boldsymbol{\beta = 100}$

$\mathbf{V_{CC}} = 2V_{CE} = 2 \text{ X } 2.5 = \mathbf{5\ V}$

Let $V_{RE} = 10\%\ V_{CC} = 0.5$ V

$R_E = V_{RE} / (I_C + I_B)$

$I_B = I_C / \beta = 1 \text{ mA} / 100 = 10\ \mu A$

$R_E = 0.5 / (1 \text{ m} + 10\ \mu) = 495\ \Omega$

Choose $\mathbf{R_E = 470\ \Omega}$

Apply KVL to collector loop

$V_{CC} - I_C R_C - V_{CE} - V_E = 0$

$R_C = (V_{CC} - V_{CE} - V_E) / I_C = (5 - 2.5 - 0.5) / 1 \text{ m}$

$R_C = 2\ k\Omega$ Choose $\mathbf{R_C = 2.2\ k\Omega}$

Let $I_{R1} = 10\ I_B = 10 \text{ X } 10\ \mu A = 100\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 0.5 = 1.1$ V (Since transistor is silicon make $V_{BE} = 0.6$ V)

$R_2 = V_{R2} / (I_{R1} - I_B) = 1.1 / (100\ \mu A - 10\ \mu A)$

$R_2 = 12.2\ k\Omega$ Choose $\mathbf{R_2 = 13\ k\Omega}$

$R_1 = (V_{CC} - V_{R2}) / I_{R1} = (5 - 1.1) / 100\ \mu A$

$R_1 = 39\ K\Omega$ Choose $\mathbf{R_1 = 38\ k\Omega}$

$X_{CE} << R_E$; $X_{CE} = R_E / 10$

$1 / (2\ \pi\ f\ C_E) = 470 / 10$ Let f = 100 Hz

$C_E = 33\ \mu F$ Choose $\mathbf{C_E = 47\ \mu F}$

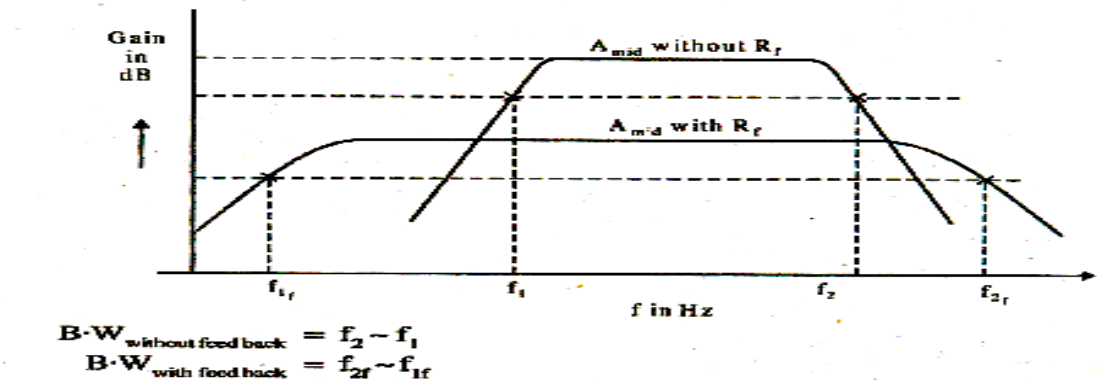
Choose $\mathbf{C_{C1} = C_{C2} = 0.1\ \mu F}$

Feedback Design:

Feedback factor $\beta = 1/80$ Feedback factor $\beta = R_B / (R_A + R_B)$

Assume $R_B = 100\ \Omega$, $\beta = 1/80$ Then $R_A = 8.3 k\Omega$

Frequency Response :



To find frequency response:

1. Connect the AC source. Keeping the frequency of the AC source in mid band region (say 10 kHz) adjust the amplitude to get the distortion less output. Note down the amplitude of the input signal.
2. Keeping the input amplitude constant, Vary the frequency in suitable steps and note down the corresponding output amplitude.
3. Calculate A_V and gain in decibels. Plot a graph of frequency Vs gain in dB. From the graph calculate f_L, f_H and bandwidth.
4. Calculate figure of merit.

To find the input impedance (Z_i) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its minimum position, apply input signal at mid band frequency (say 10 kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the input impedance.

To find the output impedance (Zo) :

1. Connections are made as shown in the diagram.
2. Keeping the DRB in its maximum position, apply input signal at mid band frequency (say 10 kHz) and adjust the amplitude of the input signal to get distortion less output. Note down the output amplitude.
3. Vary the DRB until the output amplitude becomes half of its previous value. The corresponding DRB value gives the output impedance.

Tabular Column: V_i = _____ V

f in Hz	Without Feedback			With Feedback		
	Vo in Volt	$A_V = Vo / V_i$	Gain in dB = 20*log A_V	Vo in Volt	$A_{Vf} = Vo / V_i$	Gain in dB = 20*log A_{Vf}

Result:

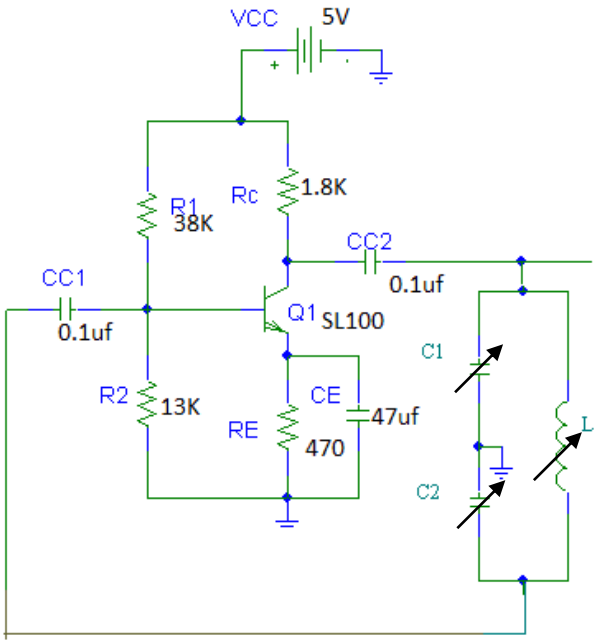
With Feedback

1. Quiescent point : V_{CE} = ____ V, I_C = _____ mA
2. Voltage Gain (A_V) = _____ (in mid band region)
3. Bandwidth (BW) = _____ Hz
4. figure of merit (FM = A_V * BW) = _____ Hz
5. Input impedance (Z_i) = _____Ω, Output Impedance (Zo) = _____Ω

Without Feedback

1. Voltage Gain (A_V) = _____ (in mid band region)
2. Bandwidth (BW) = _____ Hz
3. figure of merit (FM = A_V * BW) = _____ Hz
4. Input impedance (Z_i) = _____Ω, Output Impedance (Zo) = _____Ω

Circuit Diagram : Colpits Oscillator



Design:

Given, $\mathbf{V_{CE} = 2.5\ V}$ and $\mathbf{I_C = 1\ mA}$ Assume $\boldsymbol{\beta = 100}$

$\mathbf{V_{CC}} = 2V_{CE} = 2 \text{ X } 2.5 = \mathbf{5\ V}$

Let $V_{RE} = 10\%\ V_{CC} = 0.5$ V

$R_E = V_{RE} / (I_C + I_B)$

$I_B = I_C / \beta = 1 \text{ mA} / 100 = 10\ \mu A$

$R_E = 0.5 / (1 \text{ m} + 10\ \mu) = 495\ \Omega$

Choose $\mathbf{R_E = 470\ \Omega}$

Apply KVL to collector loop

$V_{CC} – I_C R_C – V_{CE} – V_E = 0$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C = (5 – 2.5 – 0.5) / 1 \text{ m}$

$R_C = 2\ k\Omega$ Choose $\mathbf{R_C = 1.8\ k\Omega}$

Let $I_{R1} = 10\ I_B = 10 \text{ X } 10\ \mu A = 100\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 0.5 = 1.1$ V (Since transistor is silicon make $V_{BE} = 0.6$ V)

$R_2 = V_{R2} / (I_{R1} – I_B) = 1.1 / (100\ \mu A - 10\ \mu A)$

$R_2 = 12.2\ k\Omega$ Choose $\mathbf{R_2 = 13\ k\Omega}$

$R_1 = (V_{CC} – V_{R2}) / I_{R1} = (5 – 1.1) / 100\ \mu A$

$R_1 = 39\ K\Omega$ Choose $\mathbf{R_1 = 38\ k\Omega}$

Experiment No: 3 **Date :**

Colpitts Oscillator

Aim: To design and test Hartley and Colpitts oscillator for the given frequency of oscillations crystal oscillator using BJT.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	Transistor SL 100	-	01
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DCB, DIB	-	2 each
6.	Spring board and connecting wires	-	-

Theory:

An oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave or a square wave. A **Colpitts oscillator**, named after its inventor Edwin H. Colpitts, is one of a number of designs for electronic oscillator circuits using the combination of an inductance (L) with a capacitor (C) for frequency determination, thus also called LC oscillator. One of the key features of this type of oscillator is its simplicity (needs only a single inductor) and robustness. A Colpitt's oscillator is the electrical dual of a Hartley oscillator. Fig. shows the basic Colpitt's circuit, where two capacitors and one inductor determine the frequency of oscillation. The feedback needed for oscillation is taken from a voltage divider made by the two capacitors, where in the Hartley oscillator the feedback is taken from a voltage divider made by two inductors (or a tapped single inductor).

The basic CE amplifier provides 180° phase shift and the feedback network provides the remaining 180° phase shift so that the overall phase shift is 360° to satisfy the Barkhausen criteria. The Barkhausen criteria states that in a positive feedback amplifier to obtain sustained oscillations, the overall loop gain must be unity (1) and the overall phase shift must be 0° or 360°.

When the power supply is switched on, due to random motion of electrons in passive components like resistor, capacitor a noise voltage of different frequencies will be developed at the collector terminal of transistor, out of these the designed frequency signal is fed back to the amplifier by the feedback network and the process repeats to give suitable oscillation at output terminal.

$X_{CE} << R_E$; $X_{CE} = R_E / 10 \Rightarrow 1 / (2 \pi f C_E) = 470 / 10$ Let f = 100 Hz

$C_E = 33\ \mu F$ Choose $\mathbf{C_E = 47\ \mu F}$ Choose $\mathbf{C_{C1} = C_{C2} = 0.1}$

Colpitt's oscillator: Design of tank circuit: Assume $f_o = 100$ kHz

Formula $f_o = 1 / 2\pi \sqrt{(C_T . L)}$

Where $C_T = C_1 . C_2 / (C_1 + C_2)$

Barkhausen's criterion is $A.\beta = 1$

Therefore $\beta = 1/A = C_2 / C_1$

For this circuit, A = 75 because gain of the amplifier is 75

$C_1 = 75 \cdot C_2$

Assume $C_2 = 100$pf, therefore $C_1 = 7.5$ nF, then L = 25.6 mH

Procedure:

1. Components / equipment are tested for their good working condition.
2. Connections are made as shown in the diagram
3. The quiescent point of the amplifier is verified for the designed value.
4. Observe the output wave form on CRO and measure the frequency.
5. Verify the frequency with the crystal frequency.

Application:

The Colpitt's oscillators are extensively used on all broadcast bands including the FM 88-108 MHz band.

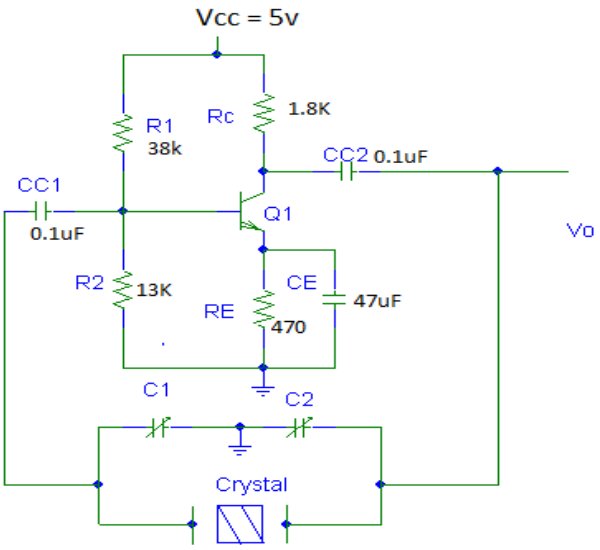
Result:

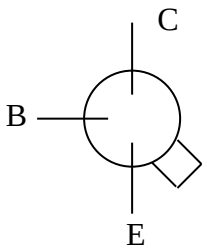
Colpitt's Oscillator:

Q Point: V_{CE} = _____ V, I_C = _____ mA, Gain (A) =_____

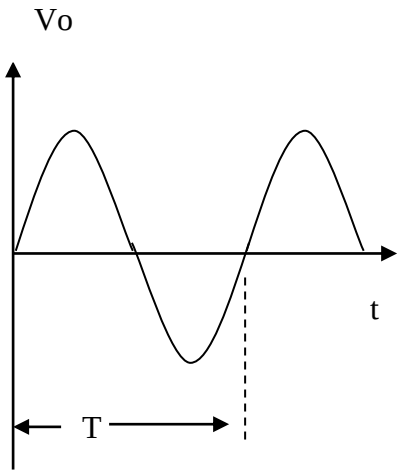
f_o Theoretical = _____ Hz, f_o Practical = _____ Hz

Circuit Diagram: Crystal Oscillator





SL100
or
CL100



$f_o = 1 / T$ Hz

Design:

Given, $\mathbf{V_{CE} = 2.5\ V}$ and $\mathbf{I_C = 1\ mA}$ Assume $\boldsymbol{\beta = 100}$

$\mathbf{V_{CC}} = 2V_{CE} = 2 \text{ X } 2.5 = \mathbf{5\ V}$

Let $V_{RE} = 10\%\ V_{CC} = 0.5$ V

$R_E = V_{RE} / (I_C + I_B)$

$I_B = I_C / \beta = 1 \text{ mA} / 100 = 10\ \mu A$

$R_E = 0.5 / (1 \text{ m} + 10\ \mu) = 495\ \Omega$

Choose $\mathbf{R_E = 470\ \Omega}$

Apply KVL to collector loop

$V_{CC} – I_C R_C – V_{CE} – V_E = 0$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C = (5 – 2.5 – 0.5) / 1 \text{ m}$

$R_C = 2\ k\Omega$ Choose $\mathbf{R_C = 1.8\ k\Omega}$

Let $I_{R1} = 10\ I_B = 10 \text{ X } 10\ \mu A = 100\ \mu A$

$V_{R2} = V_{BE} + V_E = 0.6 + 0.5 = 1.1$ V

$R_2 = V_{R2} / (I_{R1} – I_B) = 1.1 / (100\ \mu A - 10\ \mu A)$

$R_2 = 12.2\ k\Omega$ Choose $\mathbf{R_2 = 13\ k\Omega}$

$R_1 = (V_{CC} – V_{R2}) / I_{R1} = (5 – 1.1) / 100\ \mu A$

$R_1 = 39\ K\Omega$ Choose $\mathbf{R_1 = 38\ k\Omega}$

$X_{CE} << R_E$; $X_{CE} = R_E / 10 \Rightarrow 1 / (2\ \pi\ f\ C_E) = 470 / 10$ Let f = 100 Hz

$C_E = 33\ \mu F$ Choose $\mathbf{C_E = 47\ \mu F}$ **Choose** $\mathbf{C_{C1} = C_{C2} = 0.1\ \mu F}$

Experiment No: 4 **Date:**

Crystal Oscillator

Aim: To design and test a crystal oscillator.

Apparatus Required:

Sl. No.	Particulars	Range	Quantity
1.	Transistor SL 100, Crystal	-	1 each
2.	Resistors & Capacitors	As per design	-
3.	CRO Probes	-	3 Set
4.	Multi meter	-	01
5.	DCB	-	02
6.	Spring board and connecting wires	-	-

Theory:

An oscillator is an electronic circuit that produces a repetitive electronic signal, often a sine wave or a square wave. A **crystal oscillator** is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. The most common type of piezoelectric resonator used is the quartz crystal, so oscillator circuits designed around them were called "crystal oscillators".

Procedure:

1. Components / equipment are tested for their good working condition.
2. Connections are made as shown in the diagram
3. The quiescent point of the amplifier is verified for the designed value.
4. Observe the output wave form on CRO and measure the frequency.
5. Verify the frequency with the crystal frequency.

Applications:

- Quartz wristwatches – keep track of time
- Digital integrated circuits- to provide a stable clock signal
- Radio transmitters and receivers- stabilize frequencies
- Signal generators, Mobile phones and Oscilloscopes, microphones

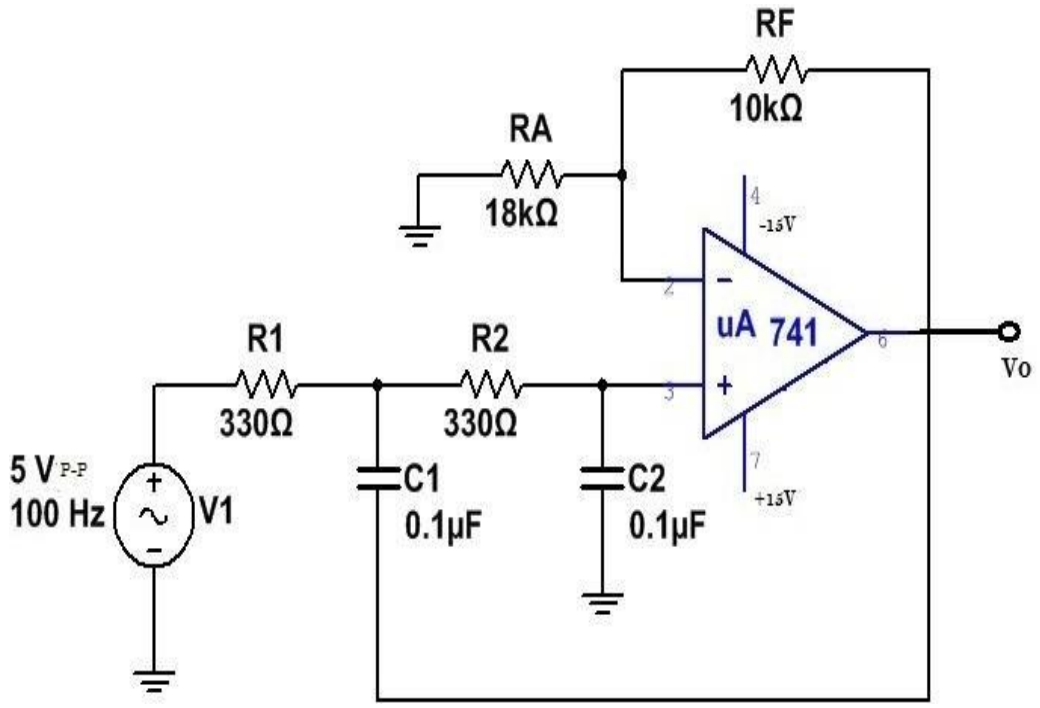
Result:

Q Point: V_{CE} = _____ V, I_C = _____ mA

f_o Crystal = _____ Hz

f_o Practical = _____ Hz

Circuit Diagram :



Design Specification: Given, Pass Band Gain (Av) = 1.586

Cut-off frequency $f_H = 5\ KHz$

i) $A_V = 1 + \frac{R_f}{R_A}$

Assume $R_f = 10\ K\Omega$

$1.586 = 1 + \frac{10\ K\Omega}{R_A} \Rightarrow R_A$ **= 17.064 *KΩ***

ii) Thecutoff frequency $f_H = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

If R1 = R2 = R and C1 = C2 = C

Then $f_H = 1 / (2\pi RC)$

Assume C = 0.1µF Then

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi X\, 5X10^{3}\, X\, 0.1X10^{-6}} = 318\ \Omega \quad (Use\ std\ 330\ \Omega)$$

So R1 = R2 = R = 330 Ω & C1 = C2 = C = 0.1µF

Experiment No: 4 **Date:**

II ORDER BUTTERWORTH ACTIVE HP AND LP FILTERS

A) Active Low Pass Filter

Aim:

To conduct an experiment to study the frequency response of an II order butterworth active low pass filter for the given design specification.

Apparatus Required:

Sl.No.	Particulars	Range	Quantity
1.	Op-amp	μA 741	01
2.	Resistors & Capacitors	As per design	-
3.	CRO + Probes	-	01 set
4.	Signal Generator	-	01
5.	Spring board + connecting wires	-	01 set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-4.
3. Apply sine wave signal of amplitude $5V_{(P-P)}$ input voltage from signal generator.
4. Vary the input frequency and note down the corresponding output amplitude.
5. Tabulate the readings and plot a graph of f (Hz) v/s gain(dB).

To find Roll off:

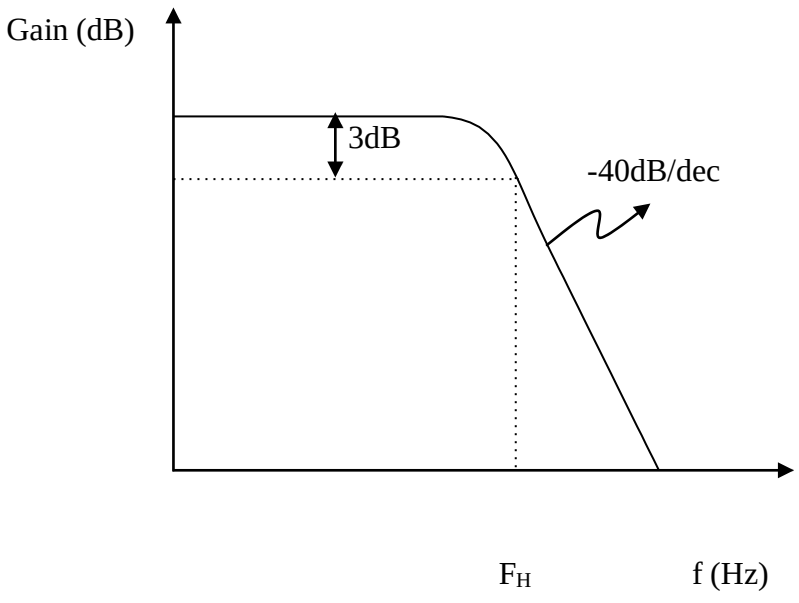
Maintaining the input signal amplitude constant, note down the output amplitude at the cut off frequency f_H and $10f_H$. The difference in the gain in dB at f_H and $10f_H$ will give the roll off.

Tabular Column:

V_i =_____V

f in Hz	Vo in Volt	Av = Vo / Vi	Gain in dB = 20 Log Av

Graph:



Result:

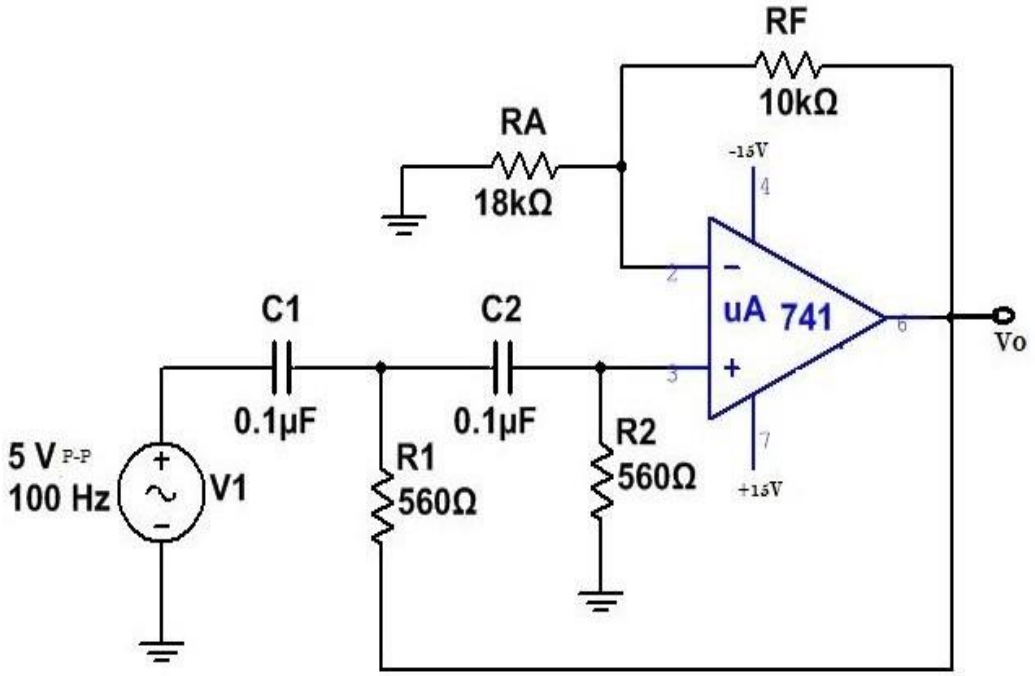
Cut off frequency, f_H Theoretical = _____

Cut off frequency, f_H Practical = _____

Pass band gain Av Theoretical = _____

Pass band gain Av Practical = _____

Circuit Diagram :



Design Specification: Given, Pass Band Gain (Av) = 1.586

Cut-off frequency $f_L = 3\ KHz$

i) $A_V = 1 + \frac{R_f}{R_A}$

Assume $R_f = 10\ K\Omega$

$1.586 = 1 + \frac{10\ K\Omega}{R_A} \Rightarrow R_A$ **= 17.064 *KΩ***

ıı) The cutoff frequency $f_L = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

If R1 = R2 = R and C1 = C2 = C

Then $f_L = 1 / (2\pi RC)$

Assume C = 0.1μF Then

$$R = \frac{1}{2\pi f_H C} = \frac{1}{2\pi X\, 5X10^3\, X\, 0.1X10^{-6}} = 530\Omega \quad (Use\ std\ 560\ \Omega)$$

So R1 = R2 = R = 560 Ω & C1 = C2 = C = 0.1μF

B) Active High Pass Filter

Aim:

To conduct an experiment to study the frequency response of an II order butterworth active high pass filter for the given design specification.

Apparatus Required:

Sl.No.	Particulars	Range	Quantity
1.	Op-amp	μA 741	01
2.	Resistors & Capacitors	As per design	-
3.	CRO + Probes	-	01 set
4.	Signal Generator	-	01
5.	Spring board + connecting wires	-	01 set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-5.
3. Apply sine wave signal of amplitude $5V_{(P-P)}$ input voltage from signal generator.
4. Vary the input frequency and note down the corresponding output amplitude.
5. Tabulate the readings and plot a graph of f (Hz) v/s gain(dB).

To find Roll off:

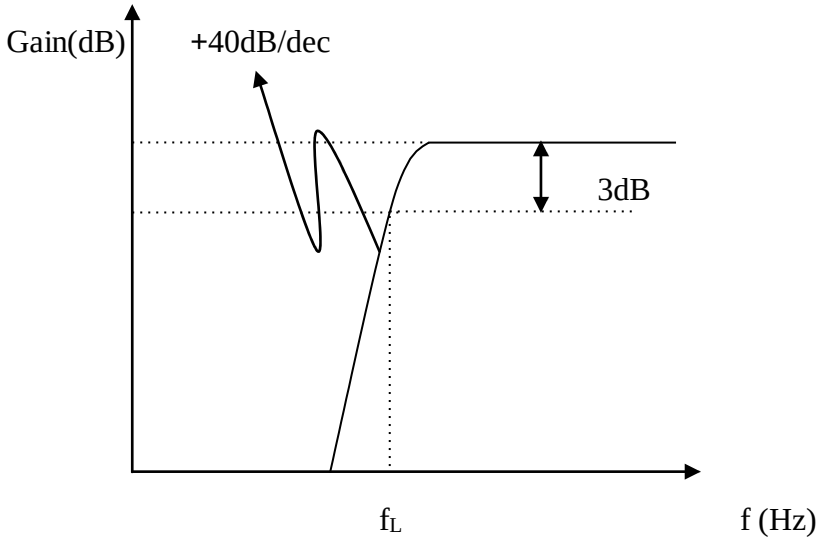
Maintaining the input signal amplitude constant, note down the output amplitude at the cut off frequency f_L and $0.1f_L$. The difference in the gain in dB at f_L and $0.1f_L$ will give the roll off.

Tabular Column :

Vi =_____V

f in Hz	Vo in Volt	Av = Vo / Vi	Gain in dB = 20 Log Av

Graph:



Result:

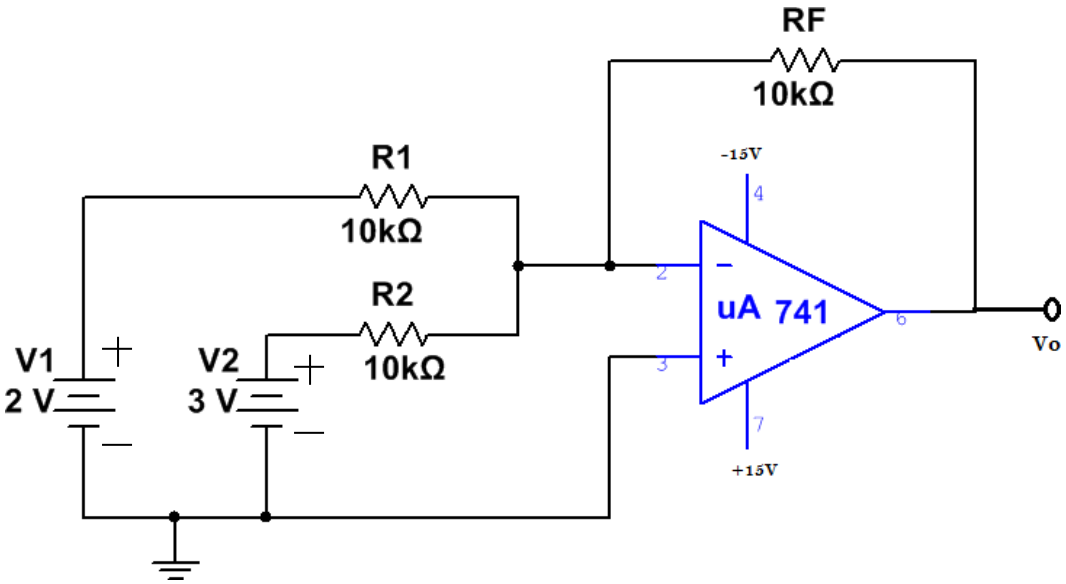
Cut off frequency, f_L Theoretical = _____

Cut off frequency, f_L Practical =_____

Pass band gain Av Theoretical =_____

Pass band gain Av Practical = _____

Circuit Diagram : Adder



Design:

Given Av=1

Let R1=R2=R=10kΩ

$$A_V = -\frac{R_F}{R};\ R_F = A_V \times R$$

R_F=10kΩ

Experiment No. 5 **Date: __ /____/ _____**

ADDER, INTEGRATOR AND DIFFERENTIATOR

A) Adder:

Aim:

To study the output and design of inverting adder using op-amp.

Apparatus Required:

Sl. No.	Particulars	Specification	Quantity
1.	Op-amp	A 741	01
2.	Resistors	As per design	-
3.	Multimeter		01
4.	Spring board + Connecting wires		01 Set

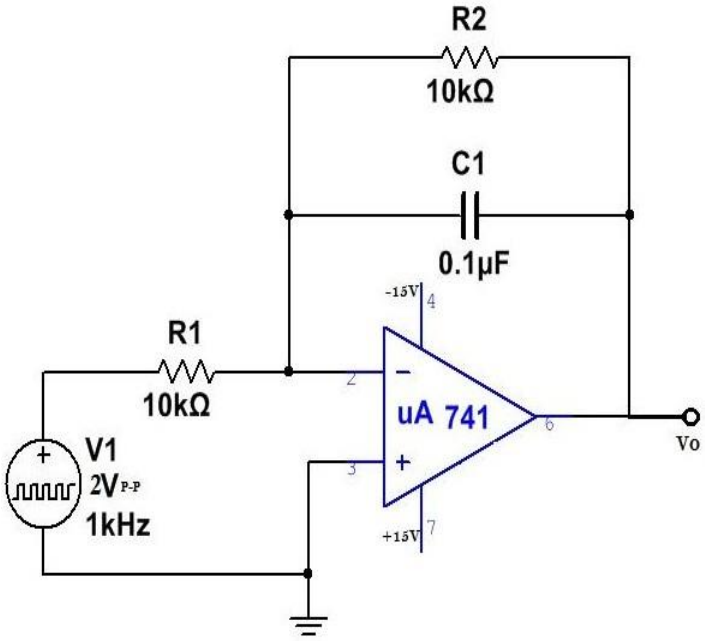
Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-8.
3. Apply input from RPS-1 (say V1=2V) and RPS-2 (Say V2=3V).
4. Observe the output from multi-meter at op-amp output pin-6.

Result:

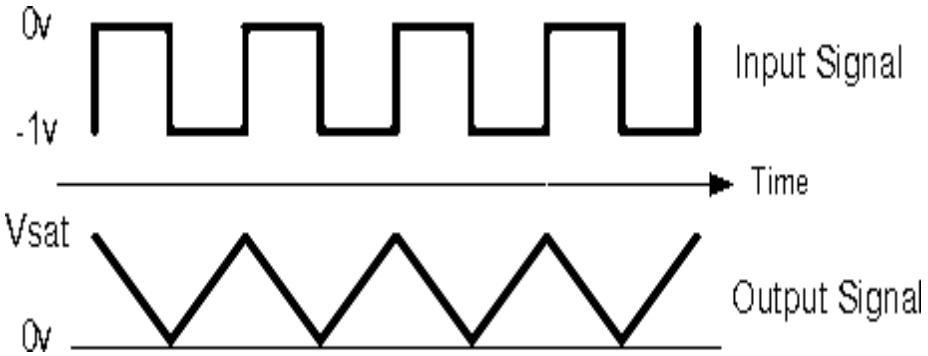
Sl. No.	Theoretical values of Vo	Practical values of Vo
1		
2		

Circuit Diagram :



$$v_o = -\frac{1}{R_1 C_F}\int_0^t v_{in}\,dt$$

Waveform:



B) Integrator:

Aim:

To study the output and design of integrator using op-amp.

Apparatus Required:

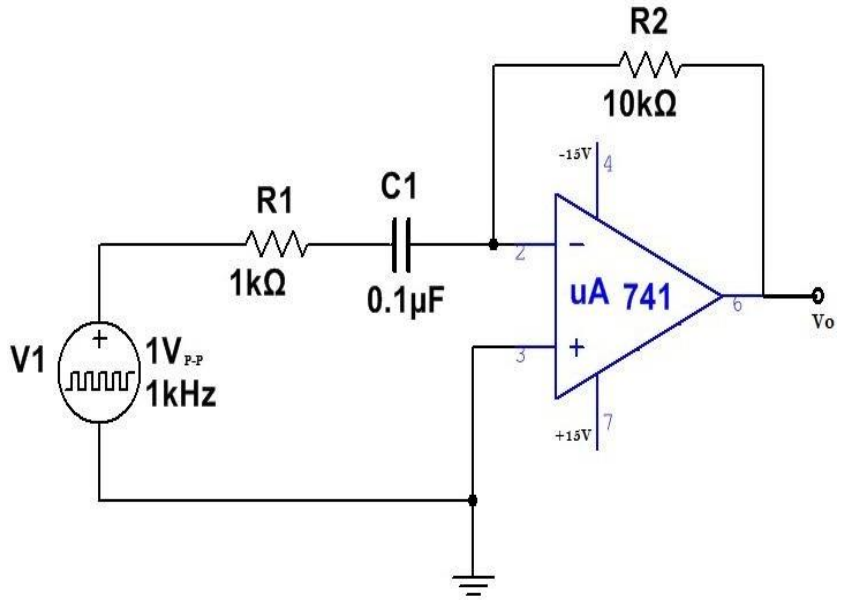
Sl. No.	Particulars	Specification	Quantity
1.	Op-amp	A 741	01
2.	Resistors and Capacitors	As per design	-
3.	CRO and Signal Generator		01 Set
4.	Spring board + Connecting wires		01 Set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-9.
3. Apply square wave input using ASG (say amplitude=$2V_{(P-P)}$ and Frequency= 1kHz).
4. Observe the output from CRO at op-amp output pin-6.

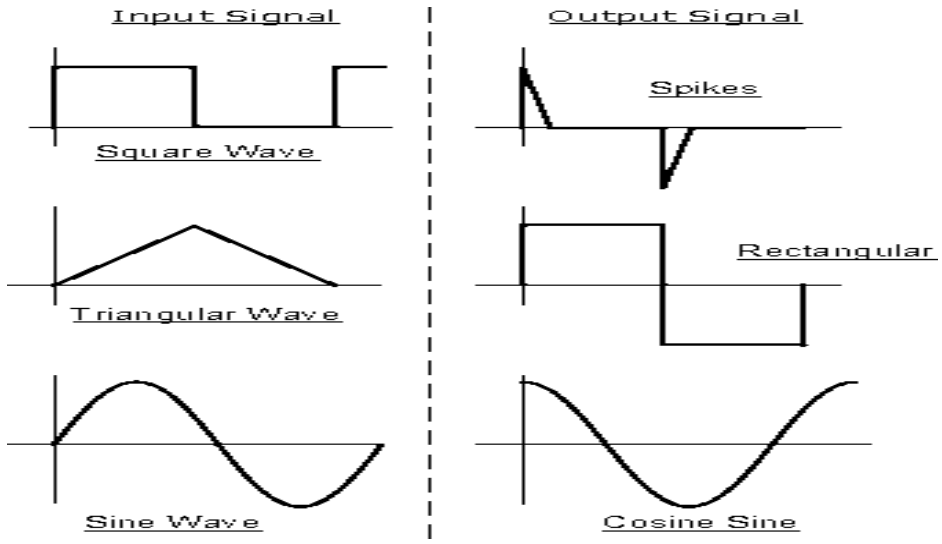
Result:

Circuit Diagram :



$$V_{\text{out}} = -RC\frac{dV_{\text{in}}}{dt}$$

Waveforms:



C) Differentiator:

Aim:

To study the output and design of differentiator using op-amp.

Apparatus Required:

Sl. No.	Particulars	Specification	Quantity
1.	Op-amp	A 741	01
2.	Resistors and Capacitors	As per design	-
3.	CRO and Signal Generator		01 Set
4.	Spring board + Connecting wires		01 Set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-9.
3. Apply Triangular wave input using ASG (say amplitude=$1V_{(P-P)}$ and Frequency= 1kHz).
4. Observe the output from CRO at op-amp output pin-6.

Result:

Design:

Case1: UTP is +ve and LTP is –ve

Let UTP = 2V LTP =-2V

We have

$$UTP = \frac{R2}{(R1+R2)}(+VSat) + \frac{R1}{(R1+R2)}\ VRef\ldots\ldots(1)$$

$$LTP = \frac{R2}{(R1+R2)}(-VSat) + \frac{R1}{(R1+R2)}\ VRef\ldots\ldots(2)$$

If UTP=LTP then ref=0

$$UTP = \frac{R2}{(R1+R2)}(+VSat), LTP = \frac{R2}{(R1+R2)}\ (-VSat)$$

+Vsat=90% Vcc=90% x12 =10.8V

$2 = \frac{R2}{(R1+R2)}$ Let R_2 = 1.2KΩ then,

R_1 = 5.28KΩ

Case2: Both UTP and LTP are +ve

Let UTP = +3V LTP = +1V

Equation (1) - (2) gives

$$UTP - LTP = \frac{R2}{(R1+R2)}(+VSat)$$

$$(3-1) = \frac{2\ R2}{(R1+R2)}(10.8V)$$

Let R_2 = 1KΩ Then R_1 = 10KΩ

Equation (1) + (2) gives

$$UTP + LTP = \frac{2\ R1}{(R1+R2)}(+VRef)$$

$$(3+1) = \frac{2\ R1}{(R1+R2)}(+VRef)$$

Substituting R_1 and R_2 in above equation V_{Ref} = +2.2V

Case3: Both UTP and LTP are -ve

Let UTP = -1V LTP = -3V

Equation (1) - (2) gives

$$UTP - LTP = \frac{R2}{(R1+R2)}(+VSat)$$

$$(-1+3) = \frac{2\ R2}{(R1+R2)}(10.8V)$$

Let R_2 = 1KΩ Then R_1 = 10KΩ

Equation (1) + (2) gives

$$UTP + LTP = \frac{2\ R1}{(R1+R2)}(+VRef)$$

$$(-1-3) = \frac{2\ R1}{(R1+R2)}(+VRef)$$

Substituting R_1 and R_2 in above equation V_{Ref} = - 2.2V

Experiment No. 6 **Date: __ /_____/ _____**

SCHMITT TRIGGER

Aim: Design of OP-AMP Schmitt Trigger Circuit given UTP and LTP values.

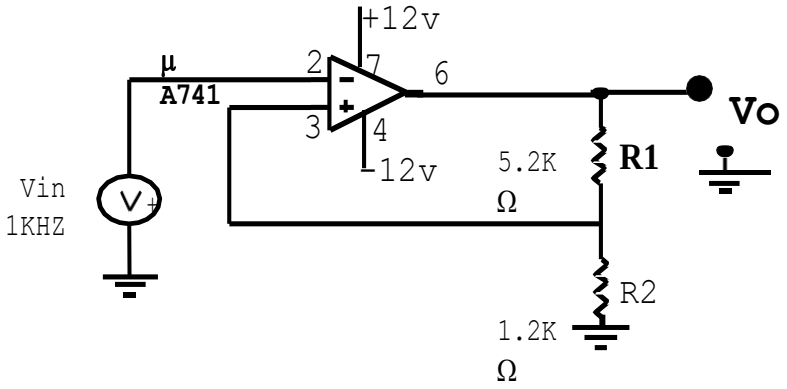
Components required:

Sl. No	Component	Range	Quantity
1	OP-AMP	A741	1
2	Resistors	1.2K, 5.28K, 1K, 10K	1-1-1-1
3	CRO, DC Power supply	--------	1,1

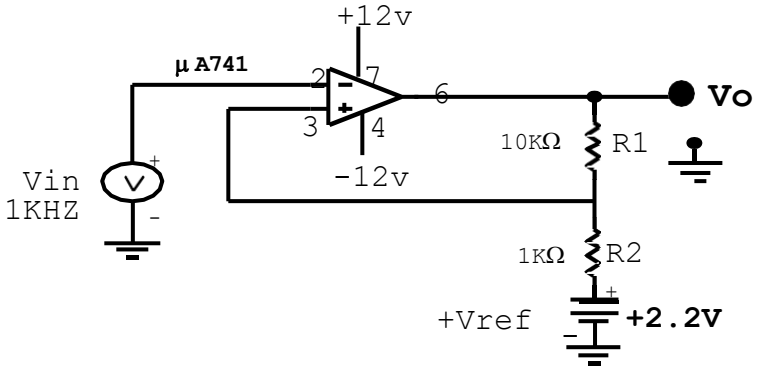
Procedure :

1. Circuit connections are made as shown in fig
2. A time varying signal is applied as input the amplitude of input voltage should be at least equal or greater than UTP or LTP. whichever is greater in magnitude of the input signal being 1KHZ.
3. Both input and output are observed simultaneously on the CRO. Input in Ac mode and output in Dc mode.
4. To get the Hysterisis Curve on CRO input signal is fed to the X channel and output is fed to Y channel of the CRO (initially X & Y channels are put to GND and the GND lines are coincides with the reference axis).**X Y** mode is pressed. The lumin Dot appearing on the screen is moved to center. Now X channel is put to Ac mode & Y channel to Dc mode .This displays the hysterisis curve from which UTP & LTP And voltages are measured and compared with the given values.

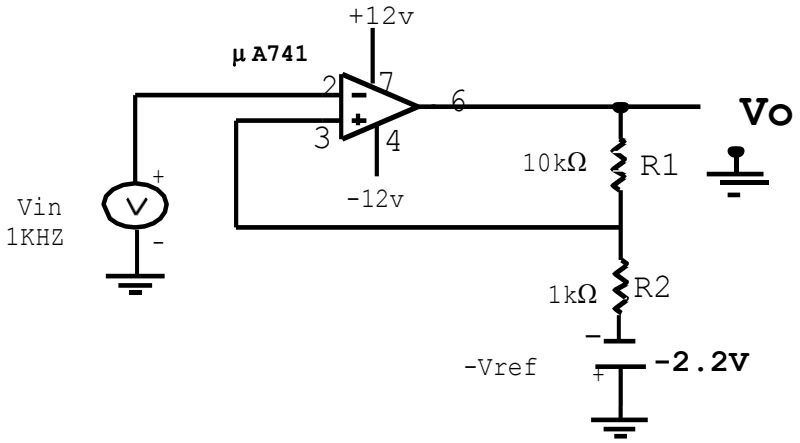
i) Without Reference Voltage:



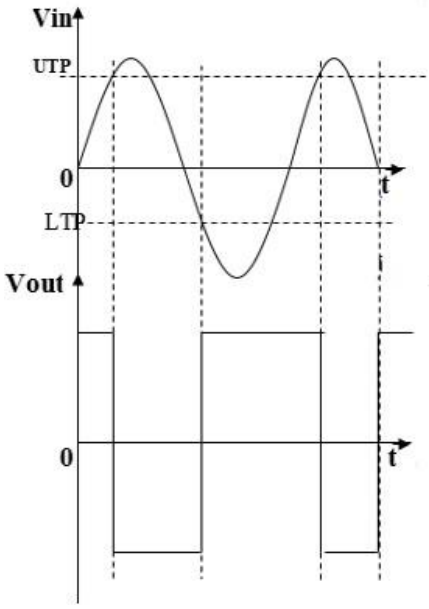
ii) With Positive Reference Voltage:



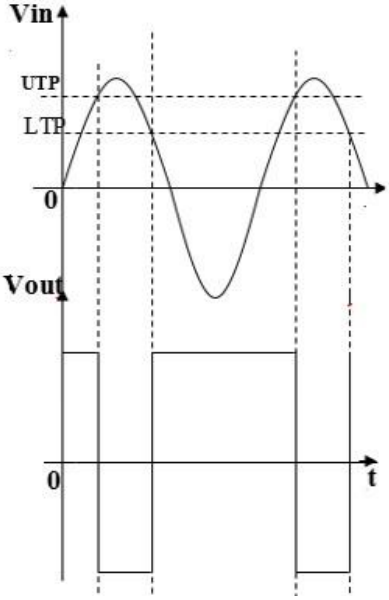
iii) With Negative Reference Voltage:



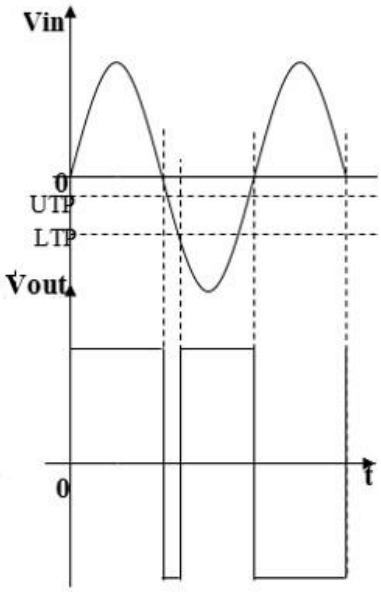
Waveforms:



Case 1 : WITHOUT REFERENCE VOLTAGE

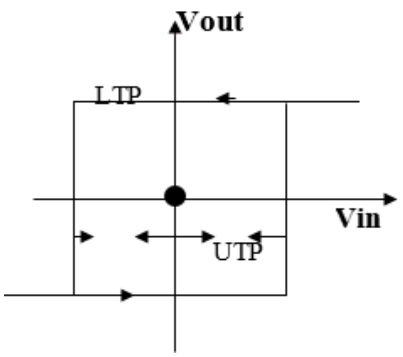


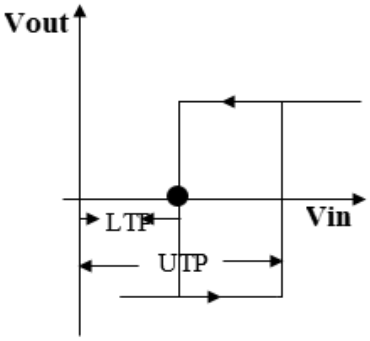
Case 2: WITH POSITIVE REFERENCE VOLTAGE

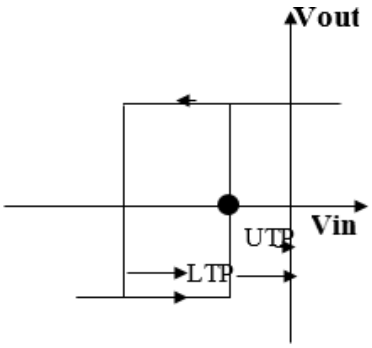


Case 3 : WITHOUT POSITIVE REFERENCE

Hysterisis Curves :



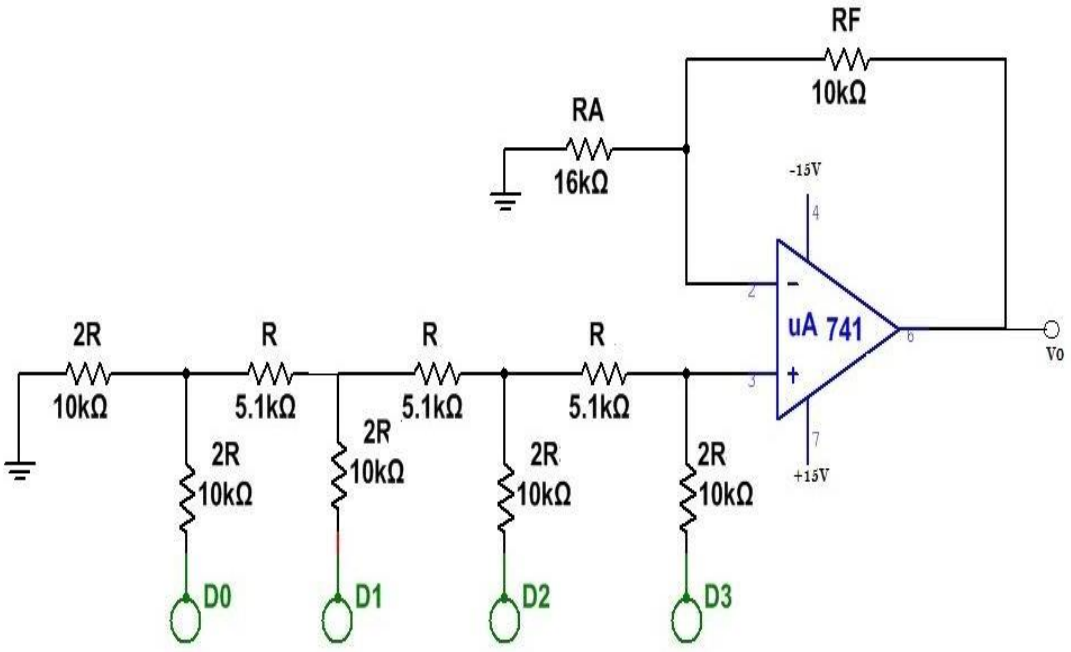




Result:

Theoretical Values		Practical Values	
UTP	LTP	UTP	LTP
+2	-2		
+3	1		
-1	-3		

Circuit diagram :



Design Specification:

Design 4 bit R-2R DAC for an output voltage, V_0 = 5V,

when the input is $(10)_d$ [i.e., $(1010)_b$].

$D_3\ D_2\ D_1\ D_0$

$(10)_{10} = (1\ \ 0\ \ 1\ \ 0)_2$

Therefore $D_3 = 1$ (MSB), $D_2 = 0$, $D_1 = 1$, $D_0 = 0$ (LSB)

$$Av = \frac{Vo}{Vi} \Rightarrow Vo = Av.Vi$$

$$Vo = \left(1 + \frac{R_F}{RA}\right)\frac{Vref}{16}(D0 + 2D1 + 4D2 + 8D3)$$

Assume RF=10kΩ, Vref=5V

$$5 = \left(1 + \frac{10k}{RA}\right)\frac{5}{16}(2 * 1 + 8 * 1)$$

RA=16kΩ

Experiment No. 7 **Date: __ /____/ _____**

4-BIT R-2R DIGITAL TO ANALOG CONVERTER

A) Given Input from Toggle Switches

Aim:

To design the four-bit DAC using op-amp from toggle switch to get the output voltage for various values of binary data.

Apparatus Required:

Sl. No.	Particulars	Specification	Quantity
1.	IC	µA741	01
2.	Resistors	As per design	-
3.	Multimeter	-	01
4.	Base board + connecting wires	-	01 Set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-6.
3. Digital input data is given at D3, D2, D1, D0 and corresponding analog output voltage V_0 is measured using voltmeter.
4. Tabulate the readings & plot the graph of V_{in} v/s V_o.

Note:

1. Do.D1.D2 & D3 are binary input.
2. V_o is the analog output.
3. Binary input Di (i = 0 to 3) can be made '0' by connecting the i/p to ground. It can be made '1' by connecting to –5 V.

   Logic 0 □ 0V

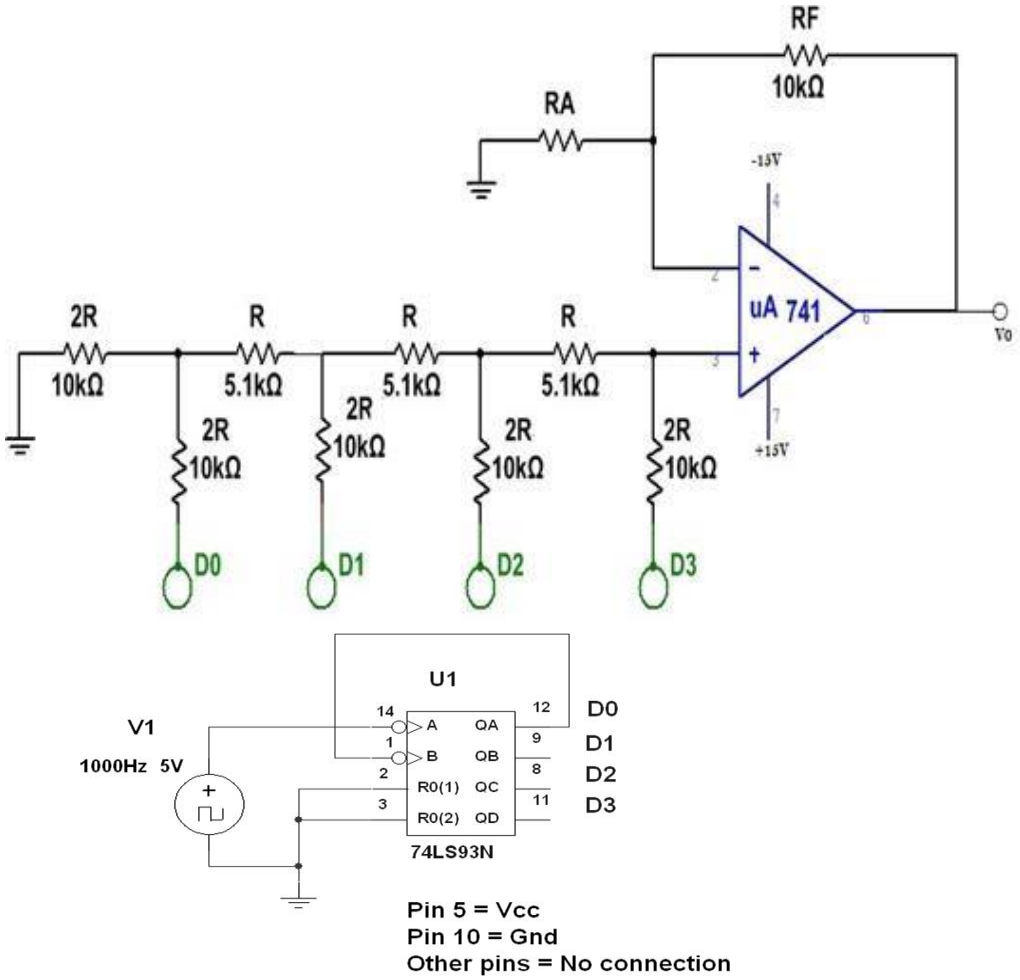
   Logic 1 □ +5V

Observation:

Decimal Value	Binary Inputs				Analog O/P Vo(volts) Theoretical values	Analog O/P Vo(volts) Practical values
	D_3	D_2	D_1	D_0		
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Result:

Circuit diagram :



Design Specification:

Design 4 bit R-2R DAC for an output voltage, V_0 = 5 V,

when the input is $(10)_d$ [i.e., $(1010)_b$].

$D_3\ D_2\ D_1\ D_0$

$(\ 10\ )_{10} = (\ 1\quad 0\quad 1\quad 0\ )_2$

Therefore $D_3 = 1$ (MSB), $D_2 = 0$, $D_1 = 1$, $D_0 = 0$ (LSB)

$$Av = \frac{Vo}{Vi} \Rightarrow Vo = Av.Vi$$

$$Vo = \left(1 + \frac{R_F}{RA}\right)\frac{Vref}{16}(D0 + 2D1 + 4D2 + 8D3)$$

Assume V_{ref}=3.3V, R_F=10KΩ

Then, R_A=7kΩ

B) Given Input from IC can work as mod-16 counter

Aim:

To design the four-bit DAC using op-amp from toggle switch to get the output voltage for various values of binary data.

Apparatus Required:

Sl. No.	Particulars	Specification	Quantity
1.	IC	µA741	01
2.	Resistors	As per design	-
3.	Multimeter	-	01
4.	Base board + connecting wires	-	01 Set

Procedure:

1. Check the components/Equipments for their working condition.
2. Connections are made as shown in the circuit diagram-7.
3. Digital input data is given at D3, D2, D1, D0 and corresponding analog output voltage V_0 is measured using voltmeter.
4. Tabulate the readings & plot the graph of V_{in} v/s V_o.

Observation:

Decimal Value	Binary Inputs				Analog O/P Vo(volts) Theoretical values	Analog O/P Vo(volts) Practical values
	D_3	D_2	D_1	D_0		
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Results :

Design :

O/p pulse width = Td = 0.5msec

For Monostable multivibrator, Td= 1.1RaC Let C=0.01μF

$0.5x10^{-3} = 1.1xR_a \times 0.01x10^{-6}$

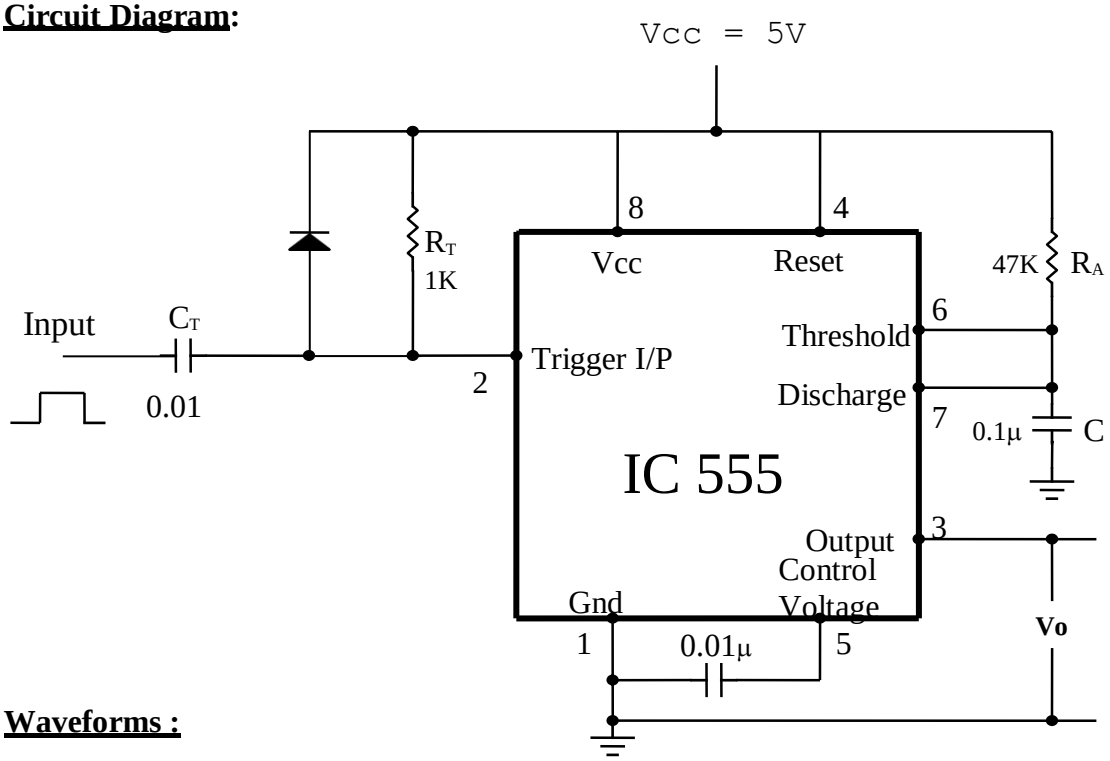
$R_a = 45.45K\Omega$, choose $R_a = 47K\Omega$ Vut ,upper threshold Vg = 2/3 Vcc Let f = 1KHz, then T = 1mSec $R_TC_T << T$

$R_TC_T = 0.1T$, Assume $C_T = 0.01\mu F$ $R_T = 0.1x1x10^{-3}/0.01x10^{-6} = 1K\Omega$

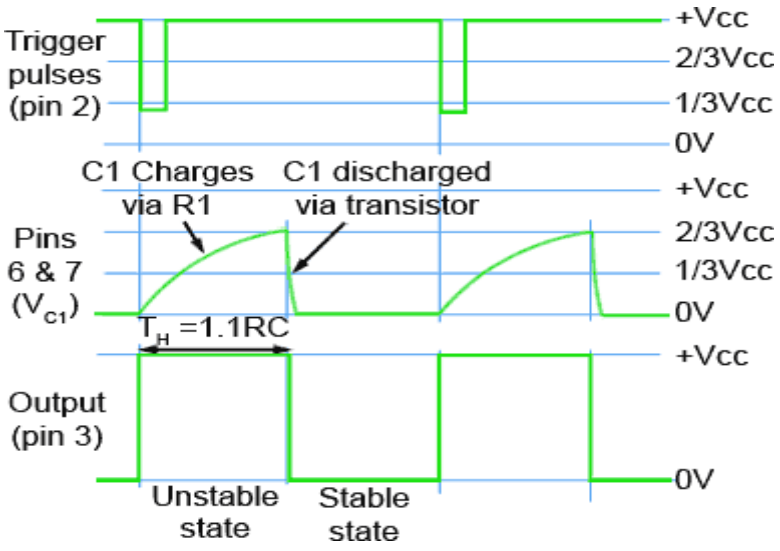
Duty cycle: D = (Td/T) x 100%

$D = (0.5x10^{-3}/1x10^{-3}) \times 100\% = 50\%$

Circuit Diagram:



Waveforms :



Experiment No.8 **MULTIVIBRATOR's** Date :

8(a): MONOSTABLE MULTIVIBRATOR

Aim : To rig up a Monostable Multivibrator using IC 555 timer to generate a pulse of given width.

Components Required :

Sl.No	Particulars	Range	Quantity
01	IC 555	------	1 No
02	Capacitor	0.1□f, 0.01□f	1each
03	Resistors	10K, 1K	1each

Procedure :

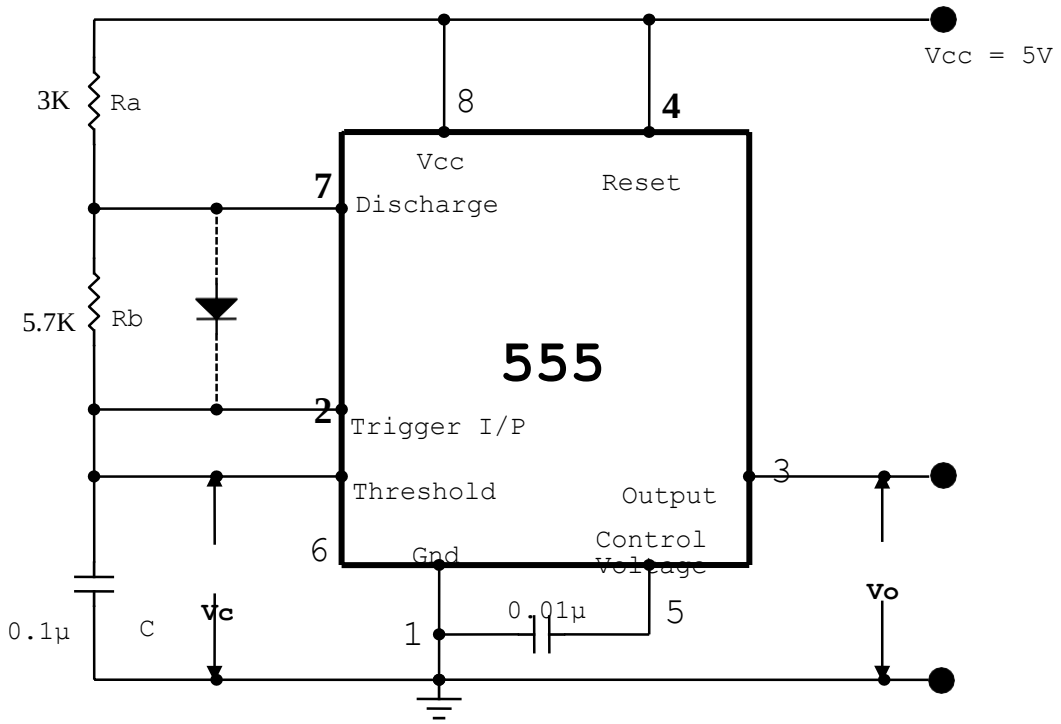
1. Connections are made as shown in the circuit diagram.
2. Trigger input pulses are applied with f = 1KHz (Square wave)
3. The pulse width of the waveforms at pin 3 is measured and verified with the designed value.
4. All voltage waveforms are observed at pin No.2,pin No.6 and Pin No.3 and traced simultaneously.

Result :

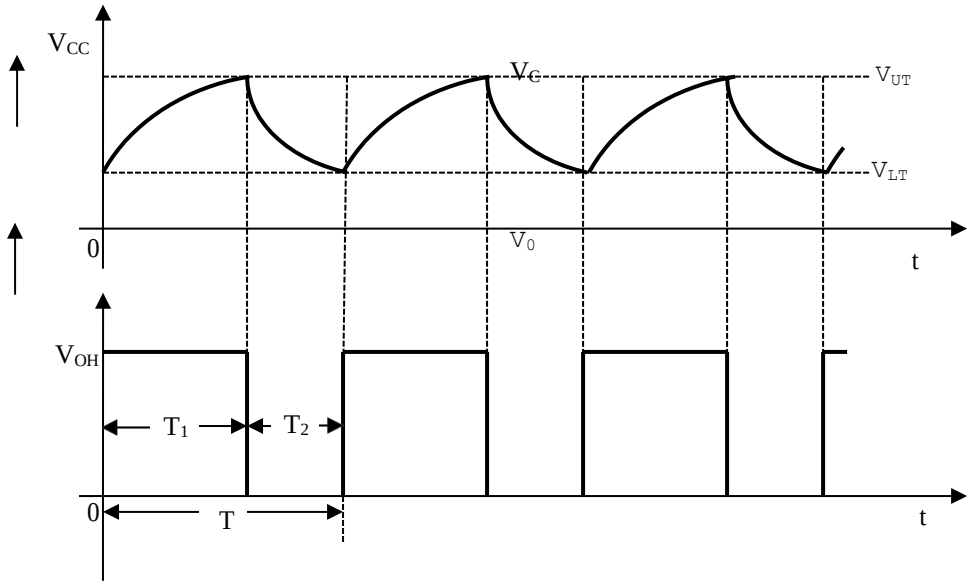
Pulse width (W) given =_____

Pulse width (W) observed = _____

Circuit Diagram:



Wave Forms:



8(b): ASTABLE MULTIVIBRATOR

Aim **:** To rig up a **Astable Multivibrator** using IC 555 timer to generate a square wave of desired frequency and duty cycle.

Component Required :

Sl.No	Particulars	Range	Quantity
01	IC 555	------	1 No
02	Capacitor	0.1□f,	2Nos
03	Resistors	5.7K□,3K□	1each
04	Resistor	7.2K□	2Nos
05	Diode	BY 127	2Nos
06	Trainer Kit	…….	…….
07	Connecting wires	…….	…….

Procedure :

1. Connections are made as shown in the circuit diagram.
2. The Ton, Toff and T of the output wave forms at pin 3 is measured and is verified with the designed value.
3. Observe the capacitor voltage waveform at pin no.6 and measure the maximum and minimum voltage levels. Verify that **VUT =(2/3)VCC** and **VLT = (1/3) VCC**.
4. Output voltage wave form is observed at pin 3

Design :

For Duty cycle 60%

Charging time
T_1=0.693*(Ra+Rb)*C Discharging time T_2=0.693*Rb*C
Let f=1 kHz and choose duty cycle = 60%
Duty cycle D = T_1/T where T = 1/f = 1mSec
T_1 = D x T = 60% x $1x10^{-3}$ = $0.6x10^{-3}$Sec
$T = T_1 + T_2$
$T_2 = T - T_1 = 1x10^{-3} – 0.6x10^{-3} = 0.4x10^{-3}$ Sec
T_2 = 0.693 x Rb x C
Assume C = 0.1µF
$Rb = T_2/(0.693xC)$
$= 0.4x10^{-3}/(0.693x0.1x10^{-6}) = 5.7K\Omega$
T_1=0.693x(Ra+Rb)xC
(Ra + Rb) = T1/(0.693xC)
$Ra = [0.6x10^{-3}/ (0.693x0.1x10^{-6})] – 5.7x10^3$
Ra = 2.95KΩ, choose Ra = 3K Ω
Note: T_1 = Ton and T_2 = Toff

For Duty cycle 50%

Charging time T_1=0.693*Ra*C
Discharging time T_2=0.693*Rb*C
Let f=1 kHz and choose duty cycle = 50%
Duty cycle D = T_1/T
where T = 1/f = 1mSec
T_1 = D x T = 50% x $1x10^{-3}$ = $0.5x10^{-3}$Sec
$T = T_1 + T_2$
$T_2 = T - T_1 = 1x10^{-3} – 0.5x10^{-3}$
Therefore, $T_2 = 0.5x10^{-3}$ Sec
T_2 = 0.693 x Rb x C
Assume C = 0.1µF
$Rb = T_2/(0.693xC)$
$= 0.5x10^{-3}/(0.693x0.1x10^{-6}) = 7.2K\Omega$
T_1=0.693 x Ra x C
Ra = T1/(0.693xC)
$Ra = 0.5x10^{-3}/ (0.693x0.1x10^{-6})$
Ra = 7.2KΩ

Result :

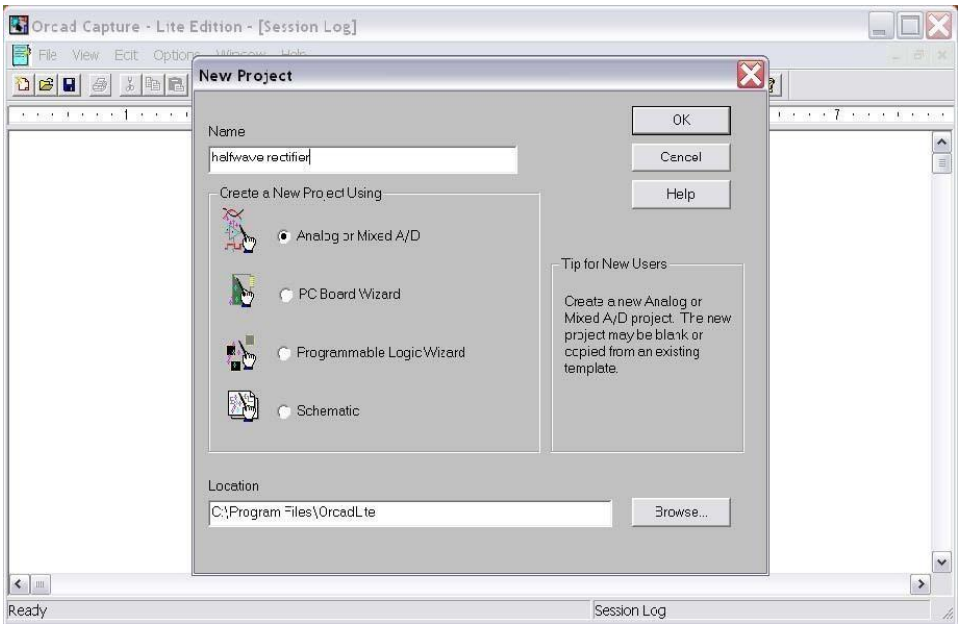
T_{on} = ------- T_{off} = ------ f = --------- Hz.

PART B : SIMULATION USING PSPICE SIMULATOR

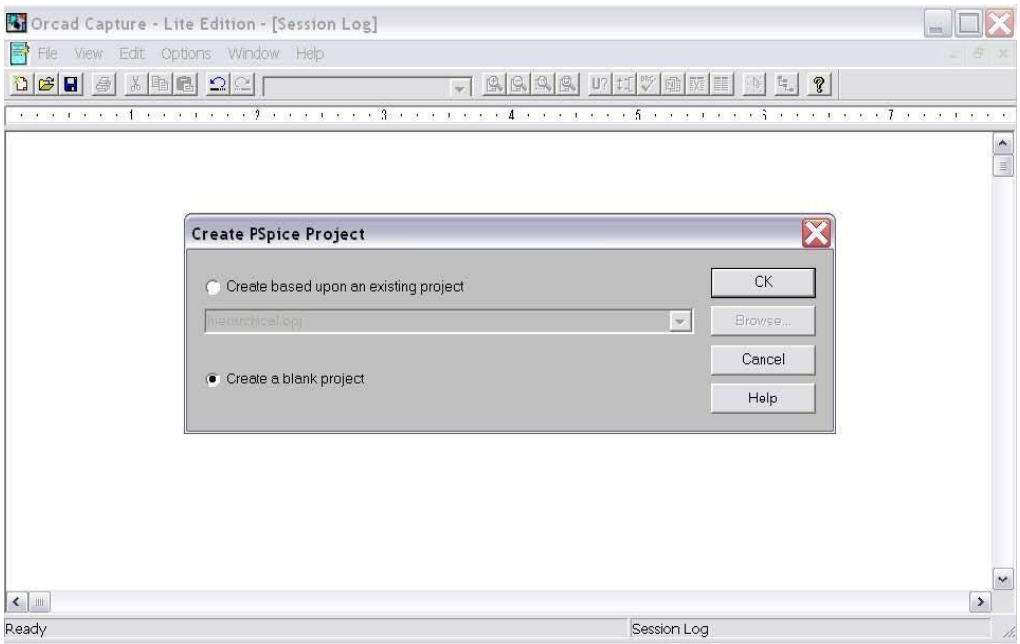
Step 1: Software opens by clicking an option "CAPTURE LITE" in the start menu.
Step 2: To start with a PSpice project:

Go to "File" menu. Select "New Project" option.

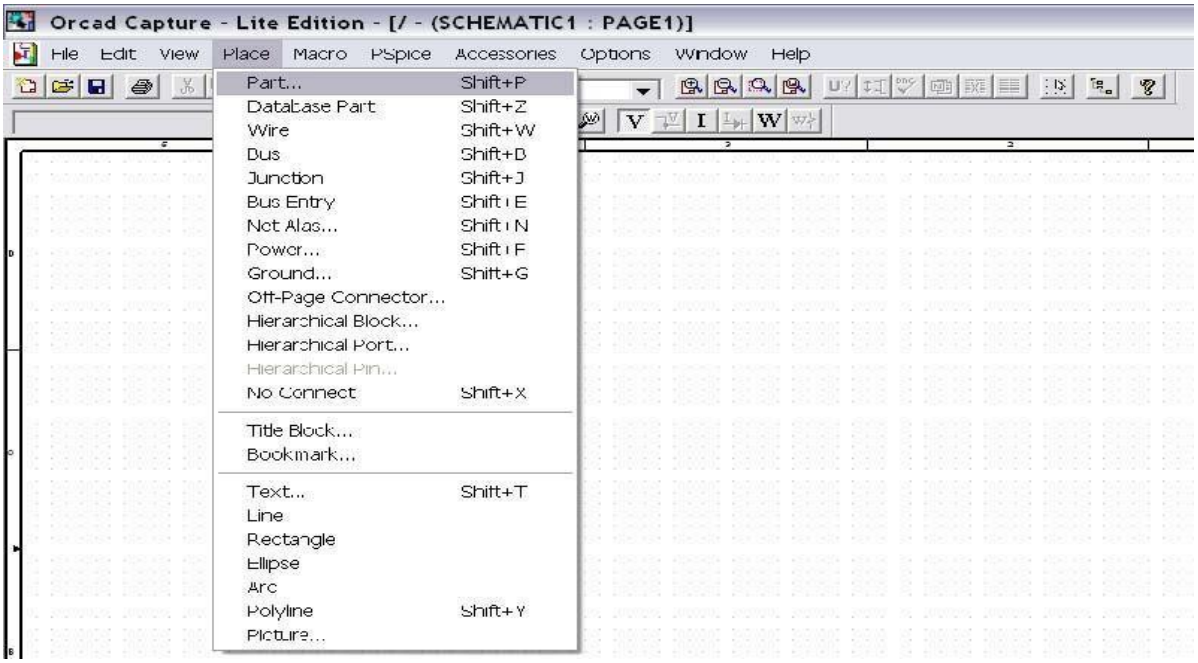
Choose "Analog or Mixed A/D" option and specify the project name and its location and click Ok



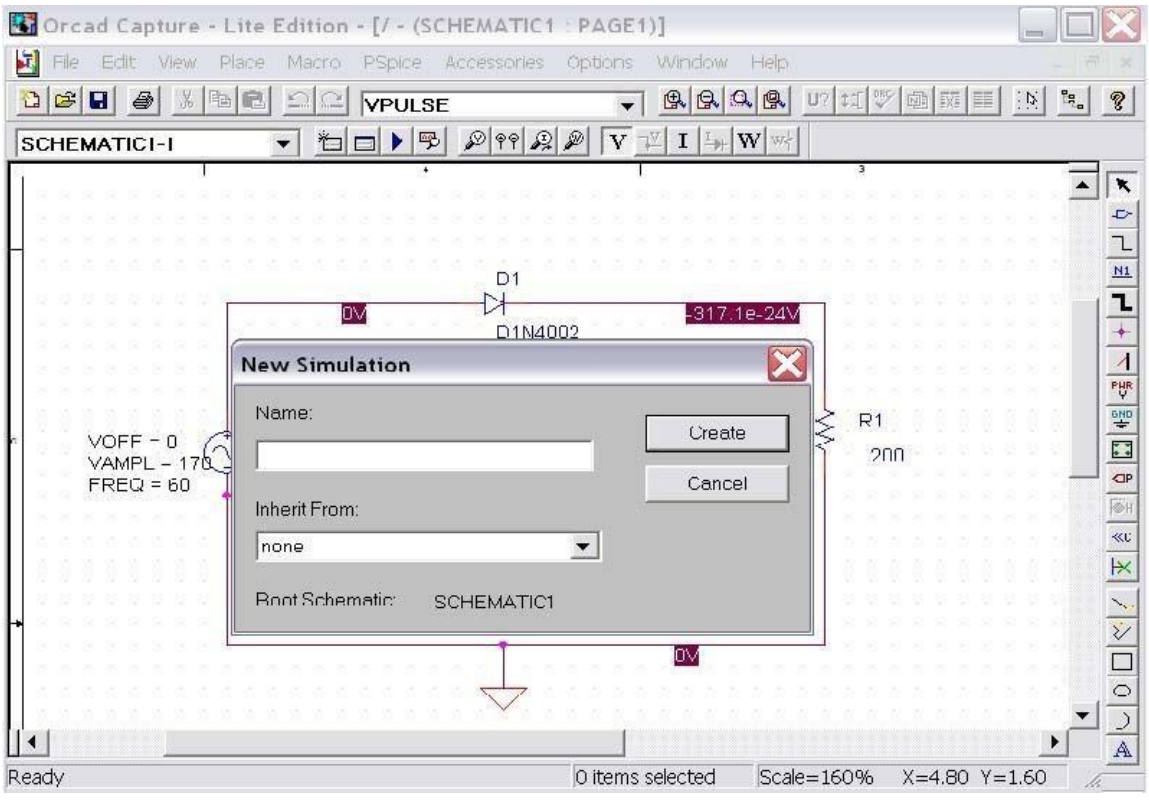
Step 3: Once the step (2) is completed the following window appears. Choose "Create a blank project" option.



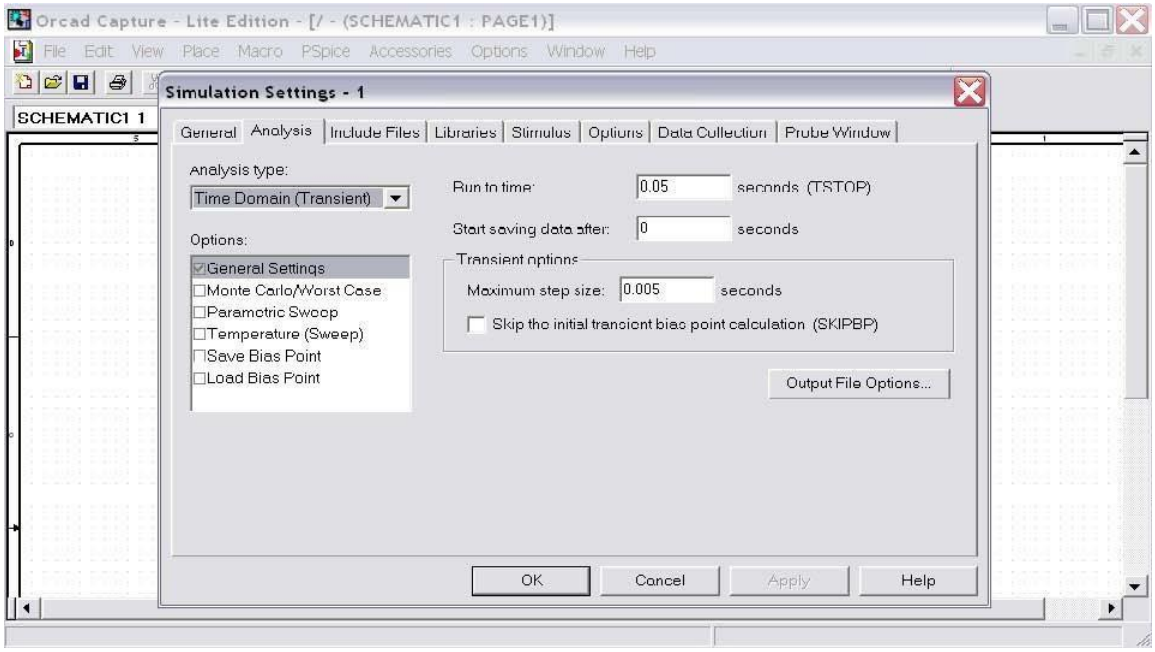
Step 4: Create the circuit by placing all its parts using "Part" option from "Place" menu. In this way a complete electrical circuit can be formed.



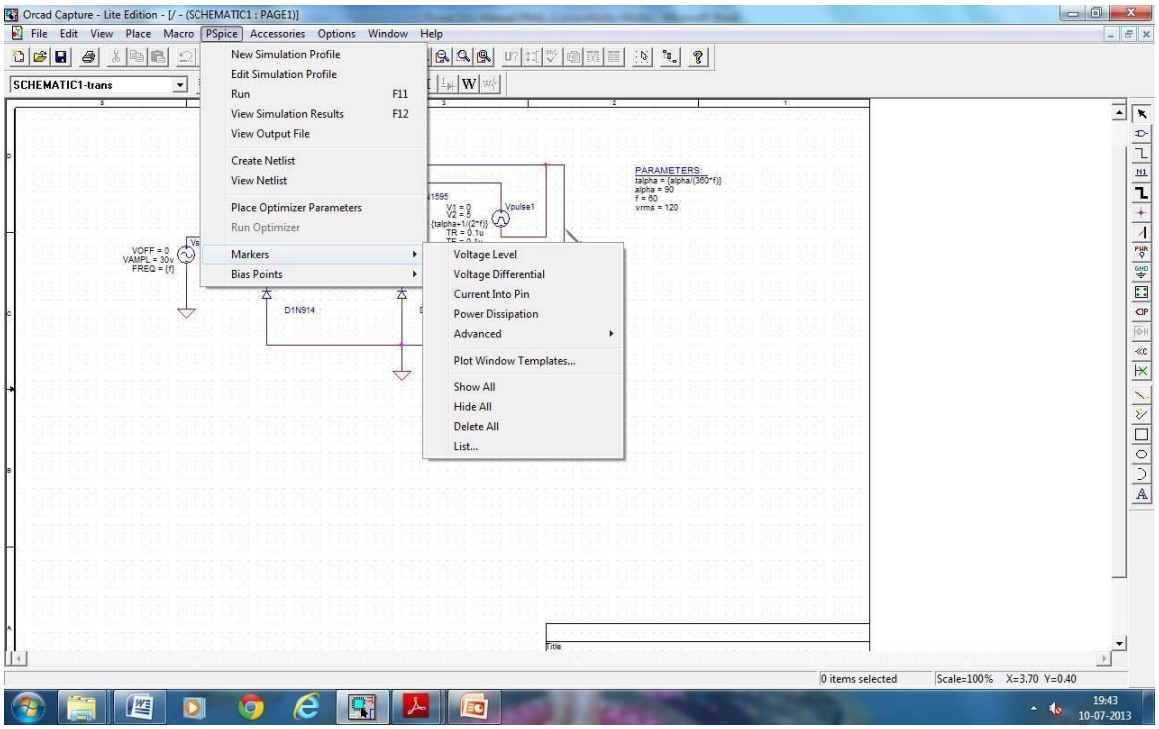
Step 5: After completing the circuit, make the simulation profile using "New Simulation Profile" command from "PSpice" menu.



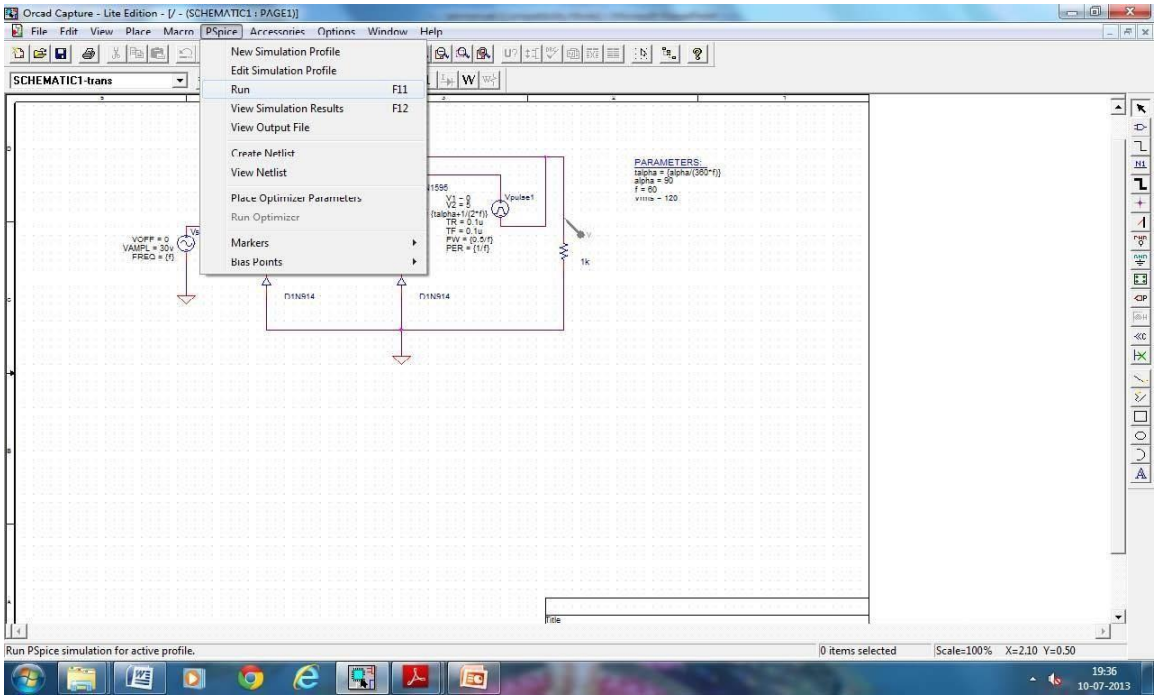
Step 6: Go to "Edit Simulation Profile" in "PSpice" menu, simulation settings window will open. Go to "Analysis" and set the simulation parameters as shown below.



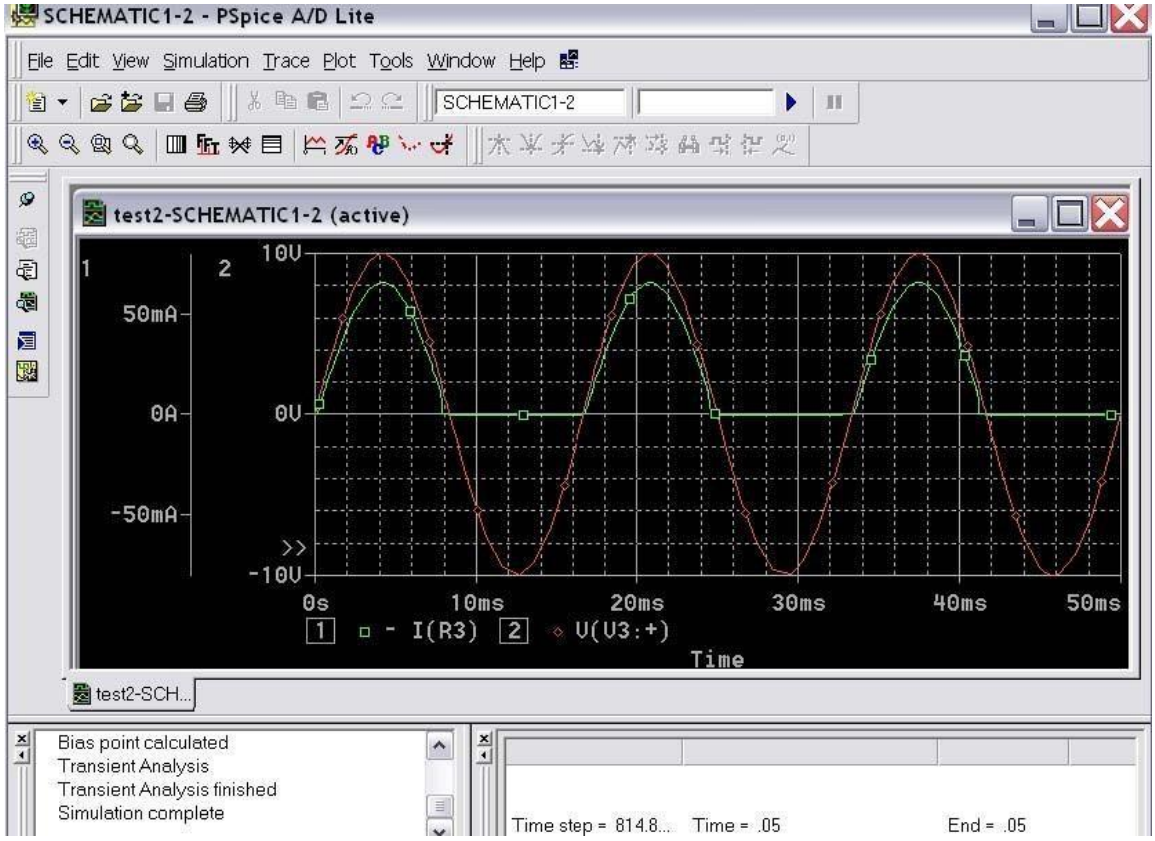
Step 7: Place the markers (voltage or current) near the required component on the circuit by using command "MARKERS" from "PSpice" menu



Step 8: Run the simulation by using command "RUN" from "PSpice" menu.



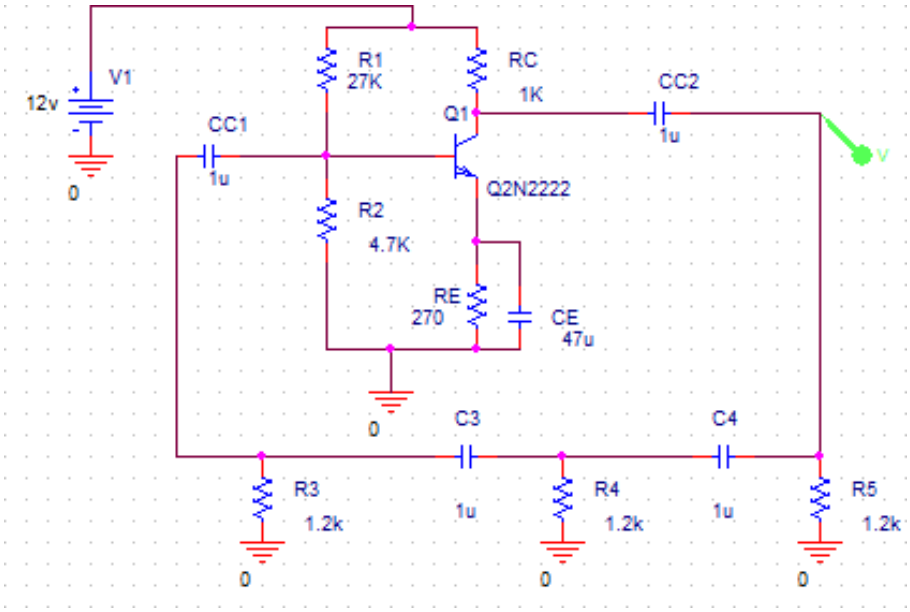
Step 9: And the results will be plotted



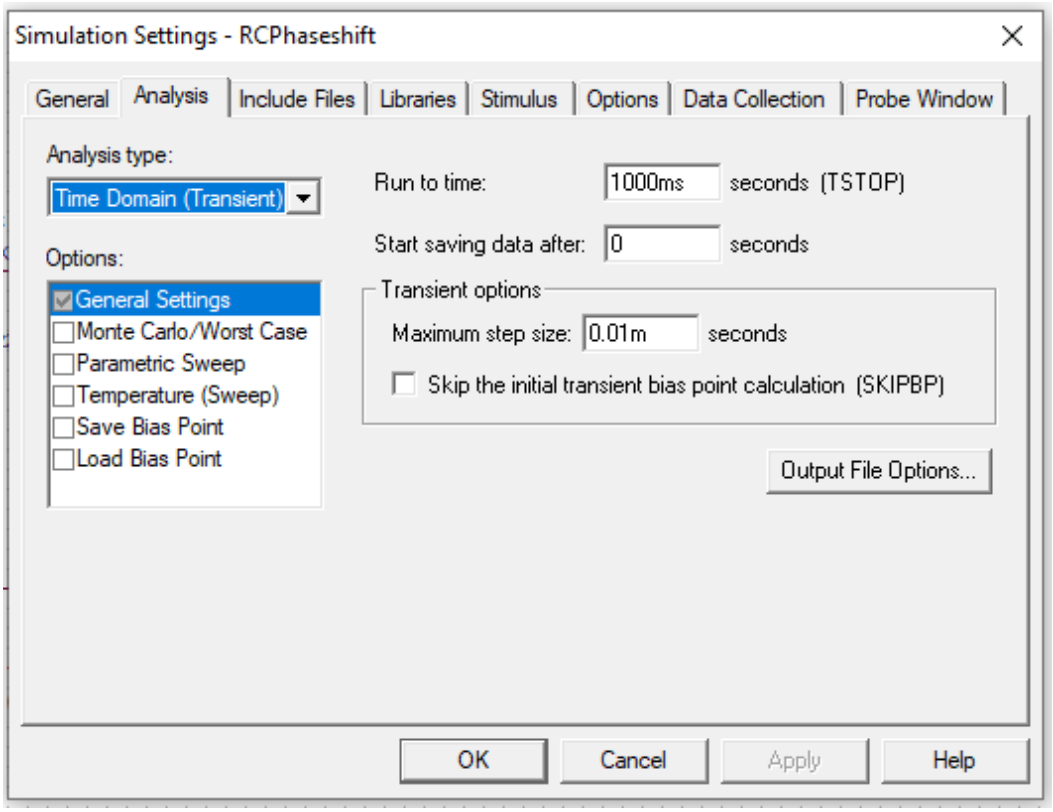
Experiment No.9:

R C PHASE SHIFT OSCILLATOR AND HARTLEY OSCILLATOR

RC PHASE SHIFT OSCILLATOR :



Simulation Profile:



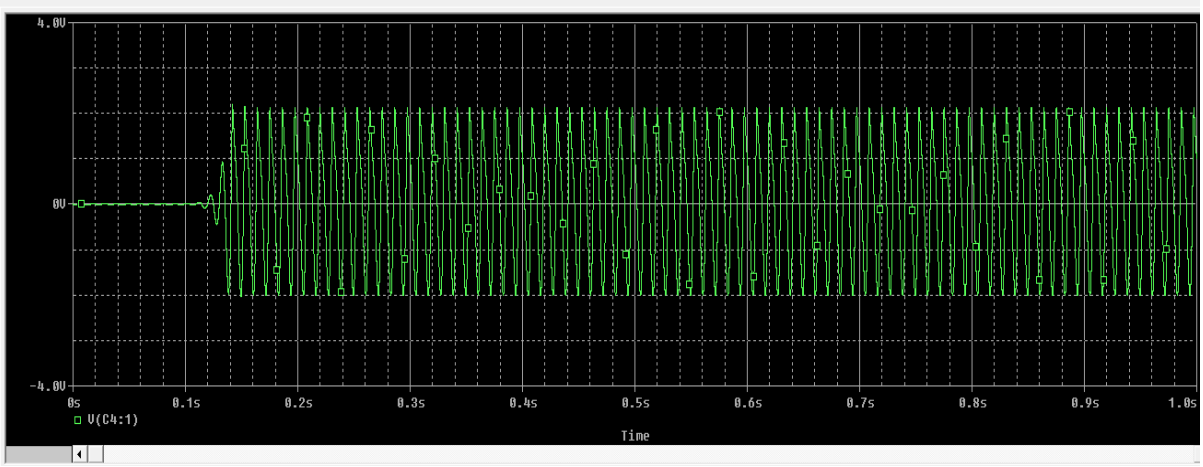
Design **:**

Use biasing circuit design which yields following values for resistors and capacitors.

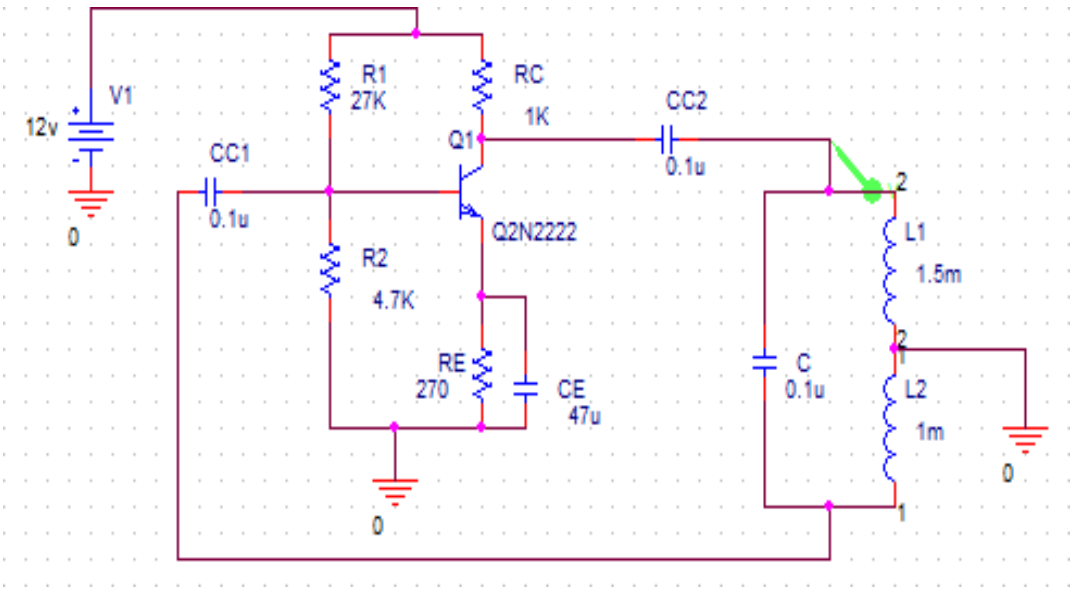
$R1 = 27K\Omega$, $R2 = 4.7K\Omega$, $R_E = 270\Omega$, $R_C = 1\ K\Omega$
$C_E = 47\mu F$ (Electrolytic), $C_C = 0.1\mu F$ (Ceramic)

$f_o = 6.5kHz$;
Assume $C = 0.01\mu F$,
$fo=1/2\pi RC\sqrt{N}$ where N = No. of stages i.e, N = 3
Then $R=1/2\pi foC\sqrt{2N} = 1/2\pi(6.5\times10^{3}\times0.01\times10^{-6}\sqrt{(2 \times 3)}) = 999.61\Omega$
Choose $R = 1K\Omega$ ($R = R_3 = R4 = R5$)

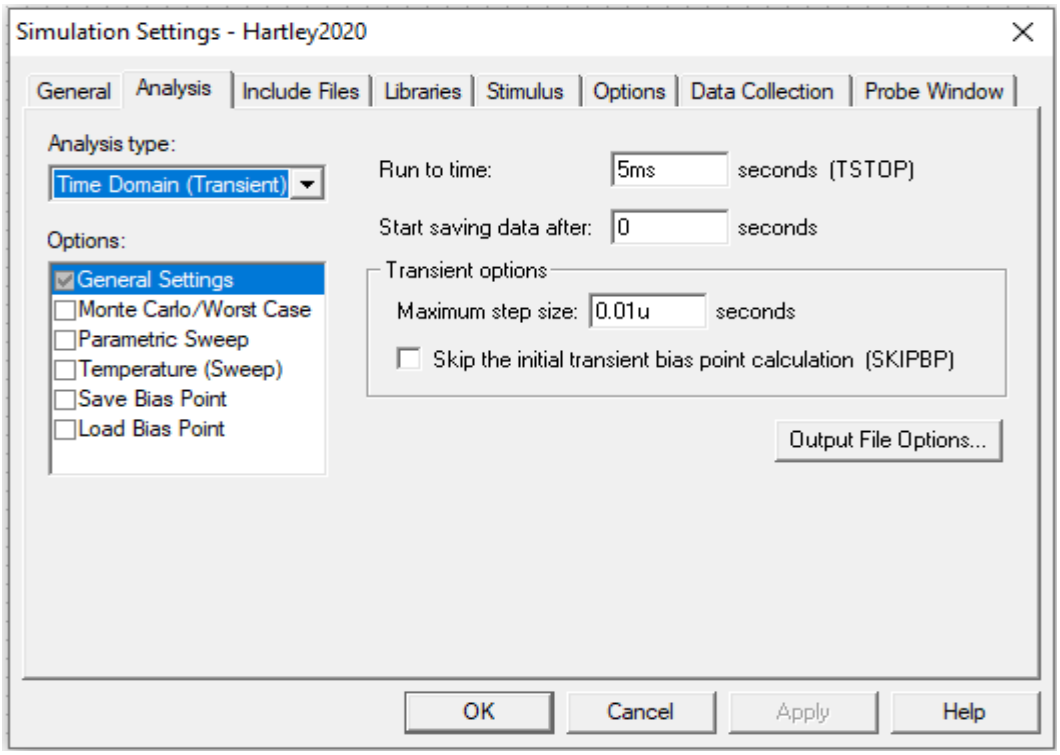
Waveform :



HARTLEY OSCILLATOR:



Simulation Profile *:*



Design:

Use biasing circuit design which yields following values for resistors and capacitors.

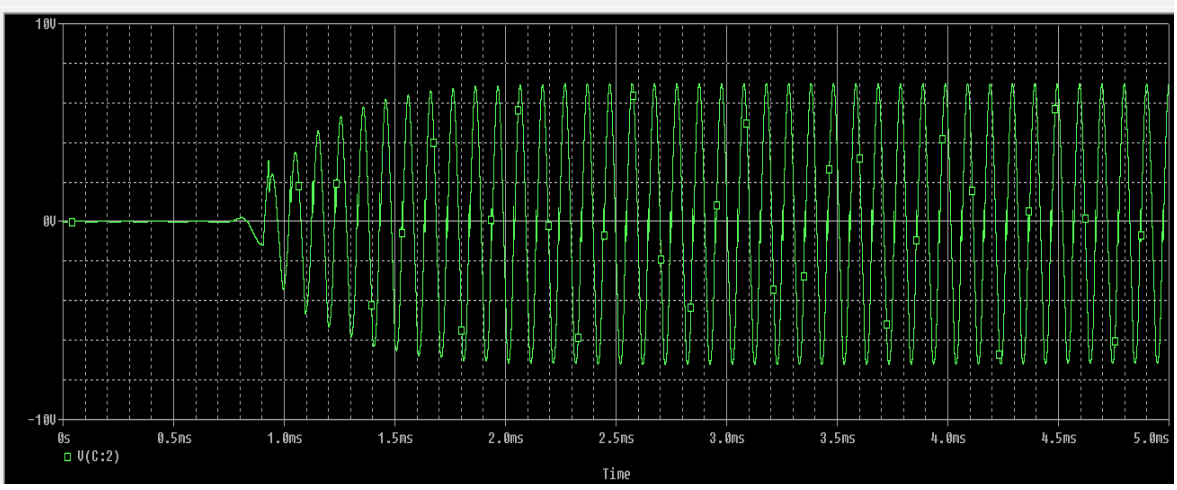
R1 = 27KΩ, R2 = 4.7KΩ, R_E = 270Ω, R_C = 1 KΩ
C_E = 47µF (Electrolytic), C_C = 0.1µF (Ceramic)

For Tank circuit:

Let f = 100KHZ and C = 1000pF

$f = \frac{1}{2\pi\sqrt{LC}}$ where $L = L_1 + L_2$ $L = \frac{1}{4\Pi^2 f^2 C}$ **= 2.53mH** **Select $L_1 > L_2$**

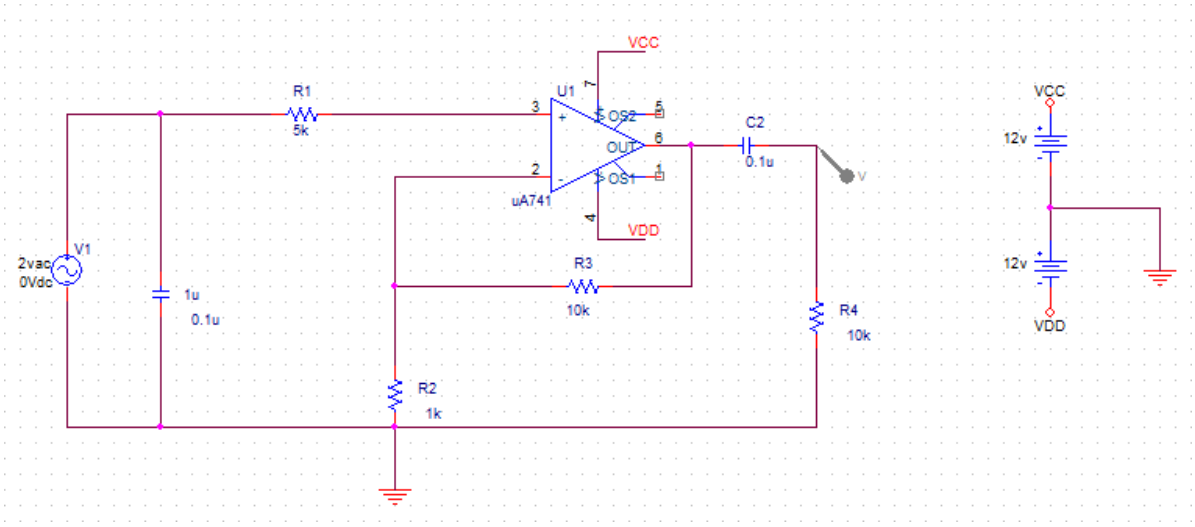
Waveform:



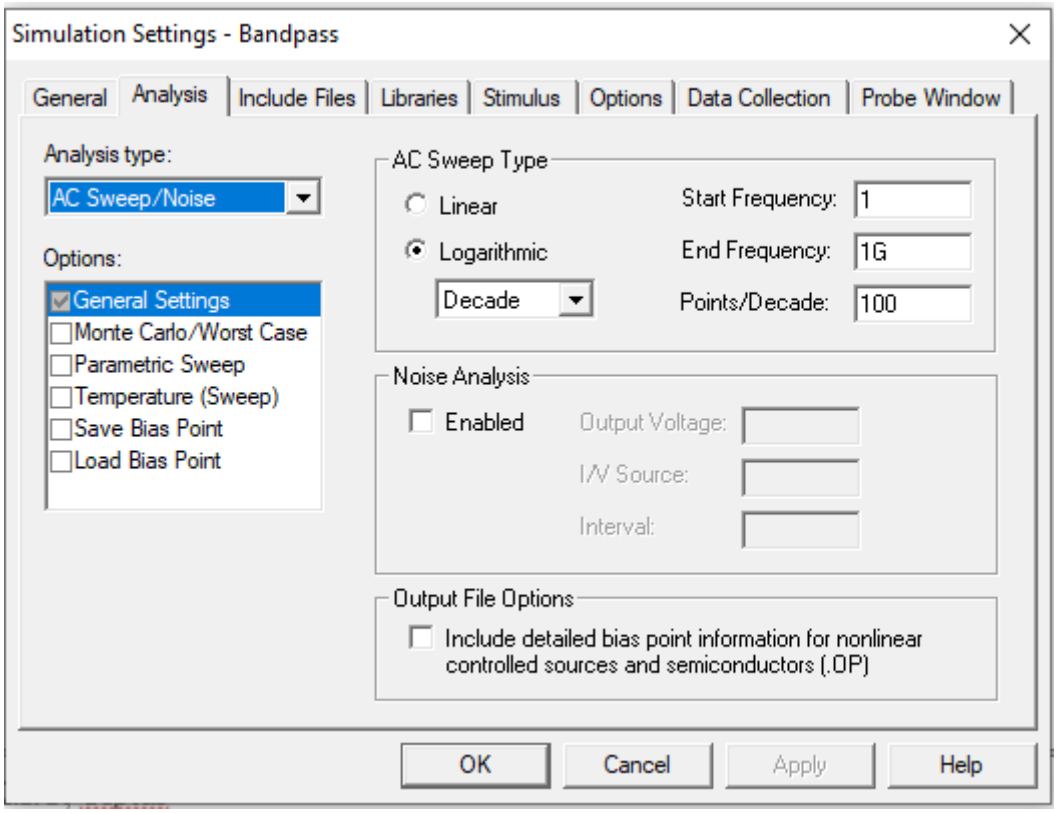
Experiment No. 10

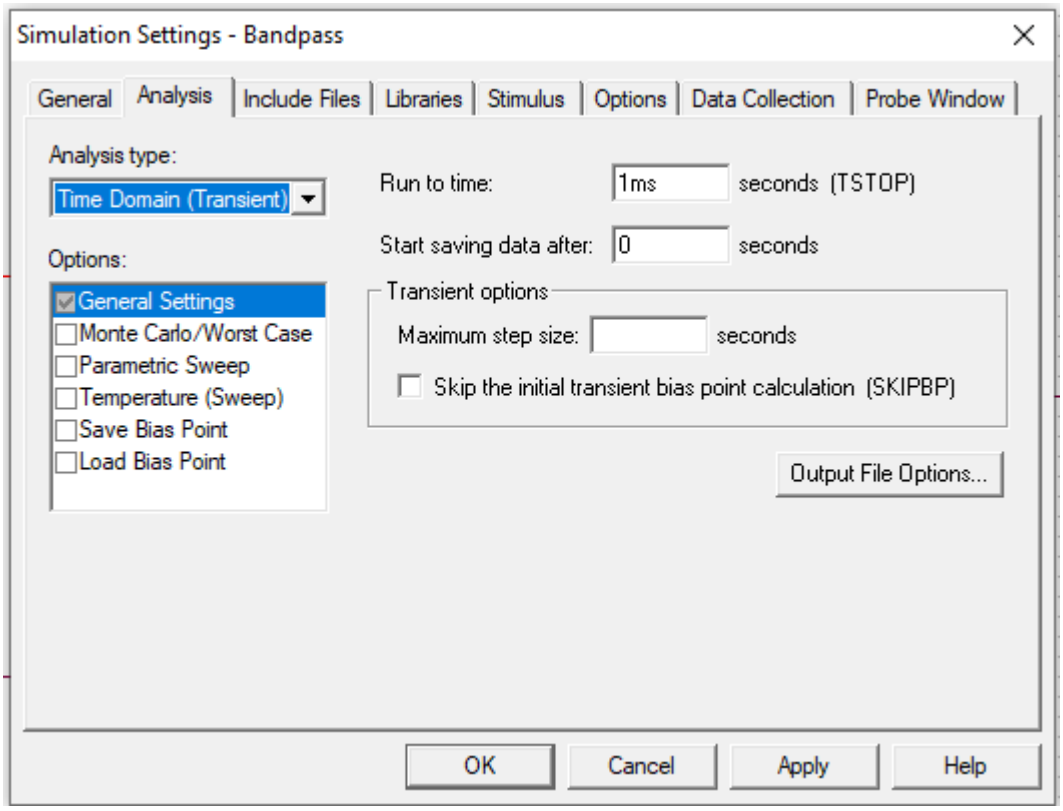
NARROW BAND PASS FILTER AND NARROW BAND REJECT FILTER

BAND PASS FILTER:



Simulation Profile :





Design :

LPF :

Let A_f =1.568 & f_c=5KHz

Af = 1 + (Rf / R1)

1.568-1 = Rf / R1

Rf =5.6 KΩ when R1=10KΩ fc = 1 / 2πRc

assume C=0.01μF

R=1 / (2π X $5x10^3$ X $0.01x10^{-6}$)

= 3.3KΩ

HPF:

Let A_f =1.568 & f_c=5KHz

Af = 1 + (Rf / R1)

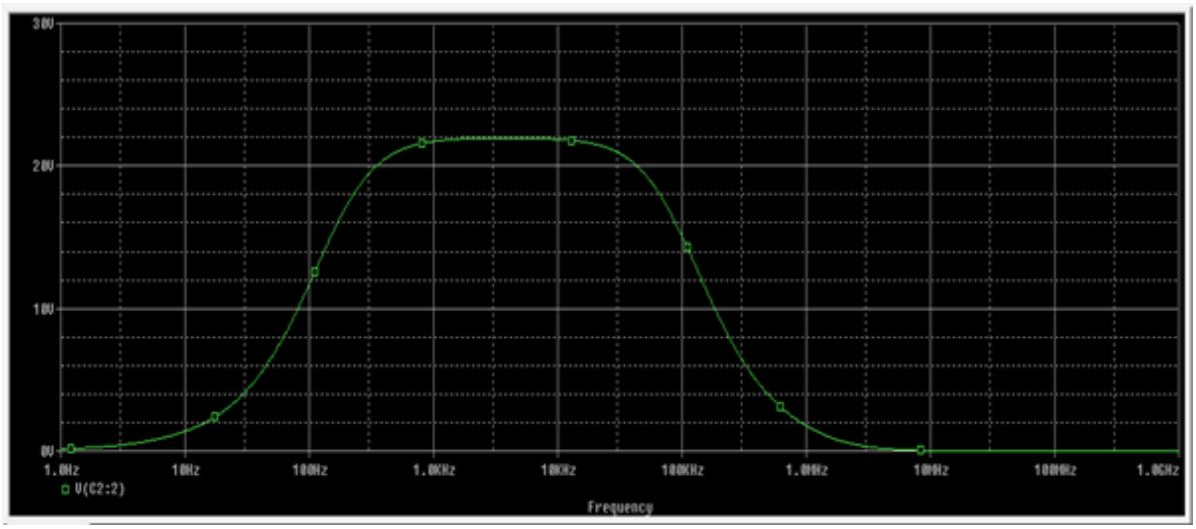
1.568-1 = Rf / R1

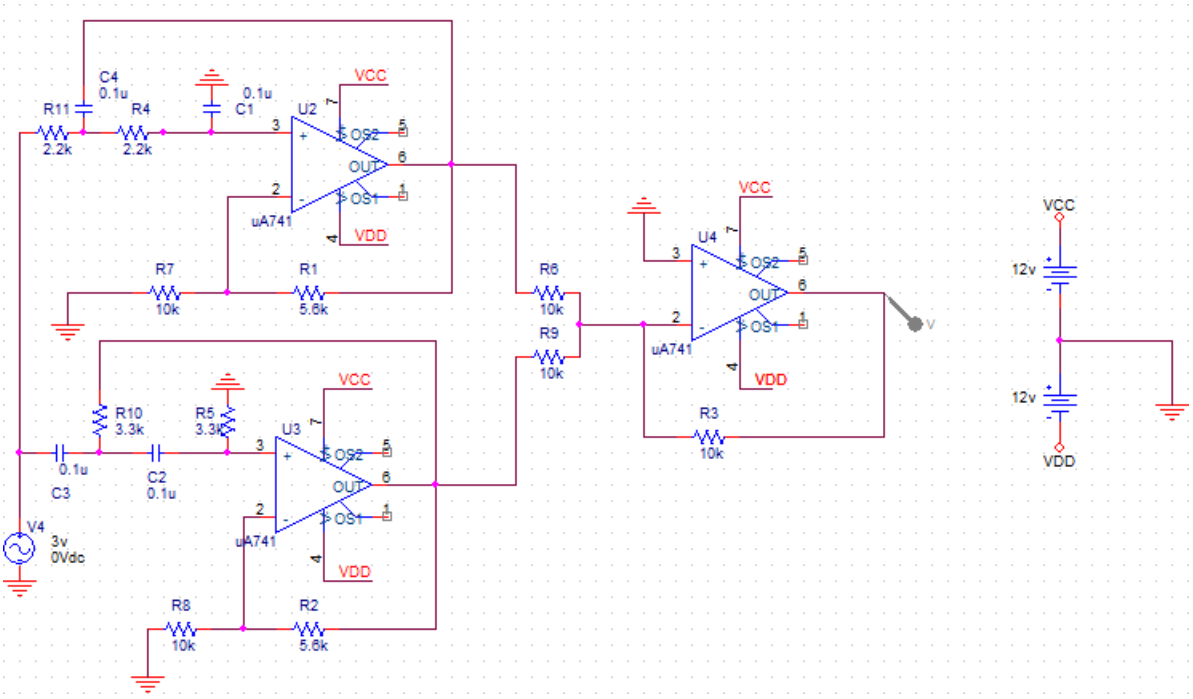
Rf =5.6 KΩ when R1=10KΩ fc = 1 / 2πRc

assume C=0.01μF

R=1 / (2π X $5x10^3$ X $0.01x10^{-6}$) = 3.3KΩ

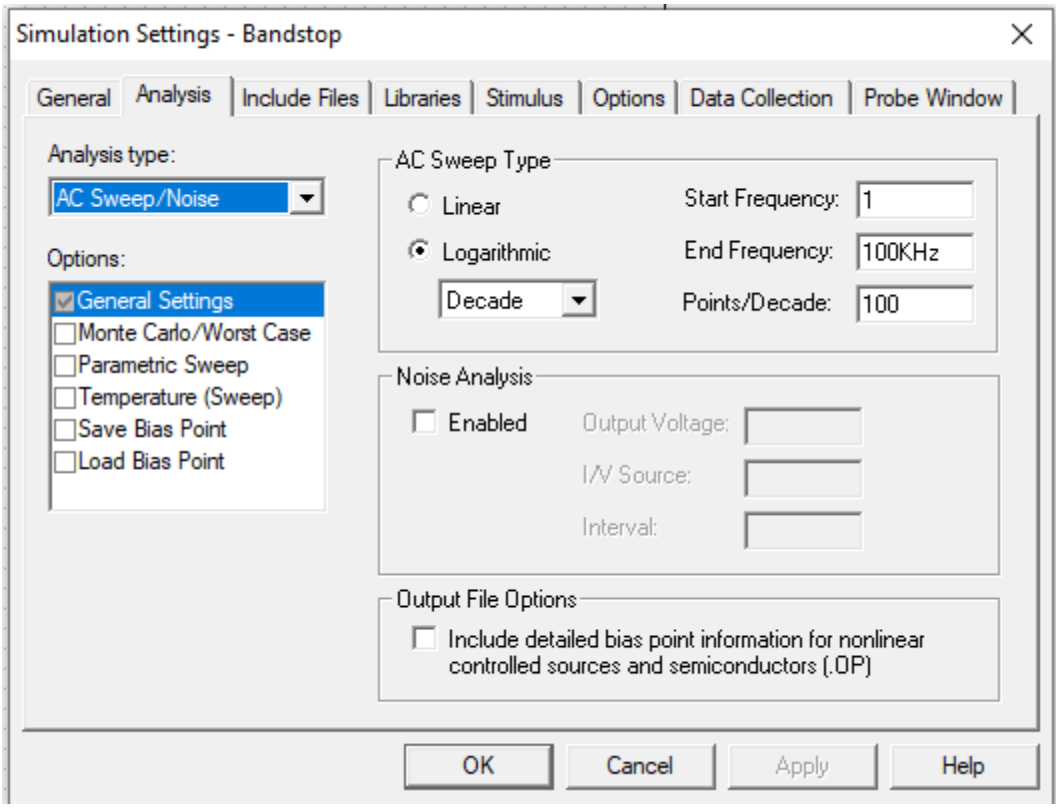
Frequency Response :

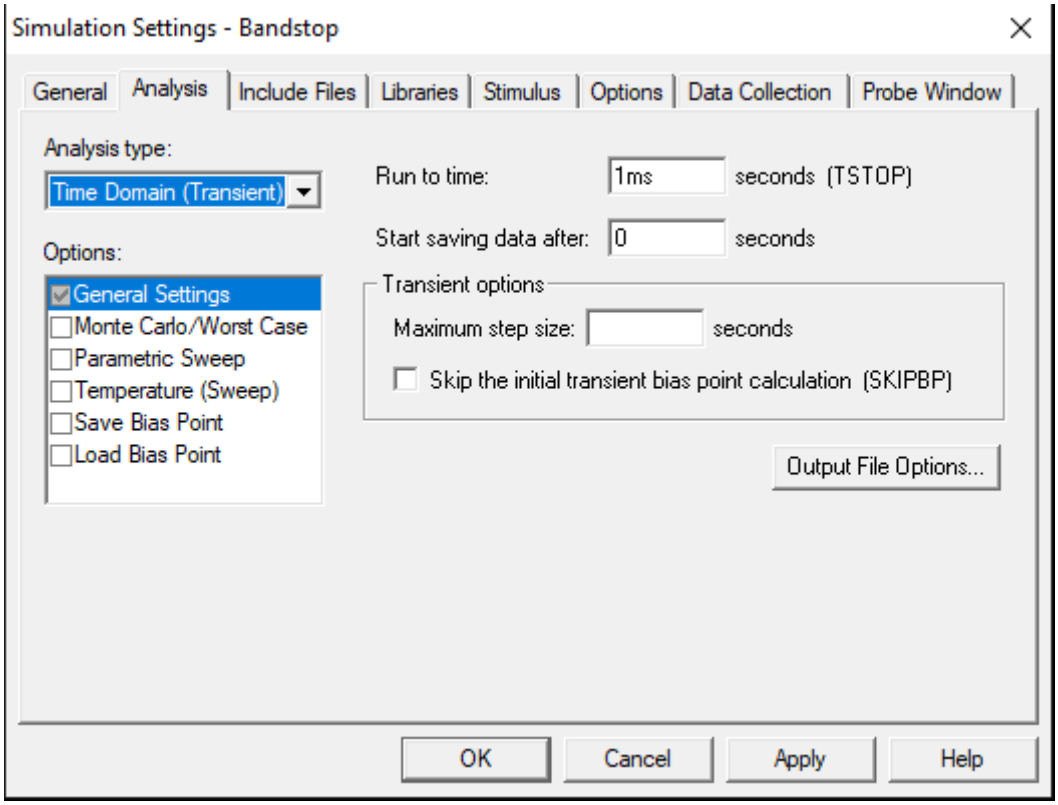




BAND REJECT FILTER:

Simulation Profile:





Design :

LPF :

Let A_f =1.568 & f_c=5KHz

Af = 1 + (Rf / R1)

1.568-1 = Rf / R1

Rf =5.6 KΩ when R1=10KΩ

fc = 1 / 2πRc

assume C=0.01μF

R=1 / (2π X $5x10^3$ X $0.01x10^{-6}$)

= 3.3KΩ

HPF:

Let A_f =1.568 & f_c=5KHz Af = 1 + (Rf / R1)

1.568-1 = Rf / R1

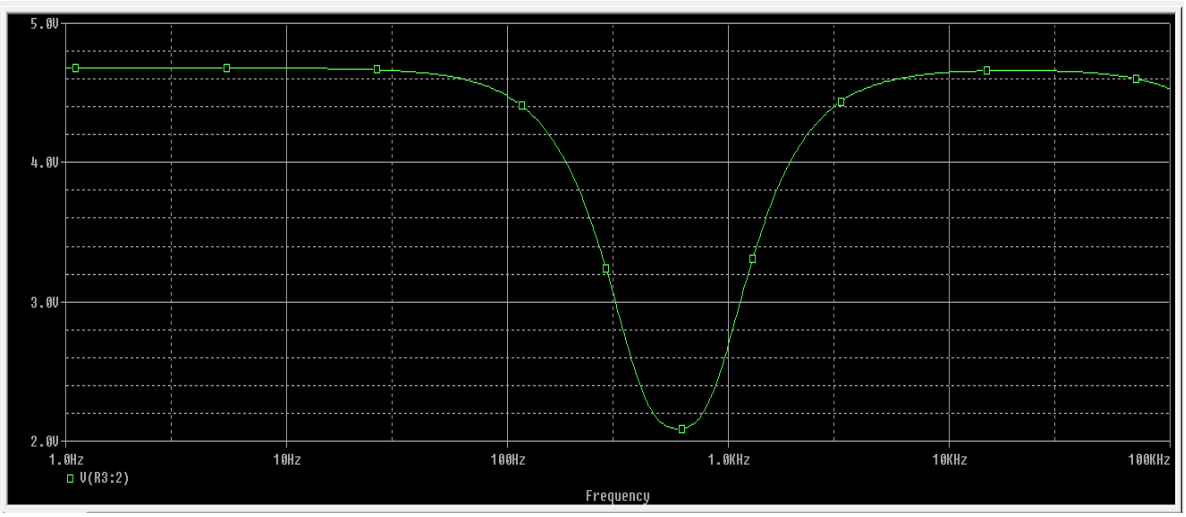
Rf =5.6 KΩ when R1=10KΩ

fc = 1 / 2πRc

assume C=0.01μF

R=1 / (2π X $5x10^3$ X $0.01x10^{-6}$) = 3.3KΩ

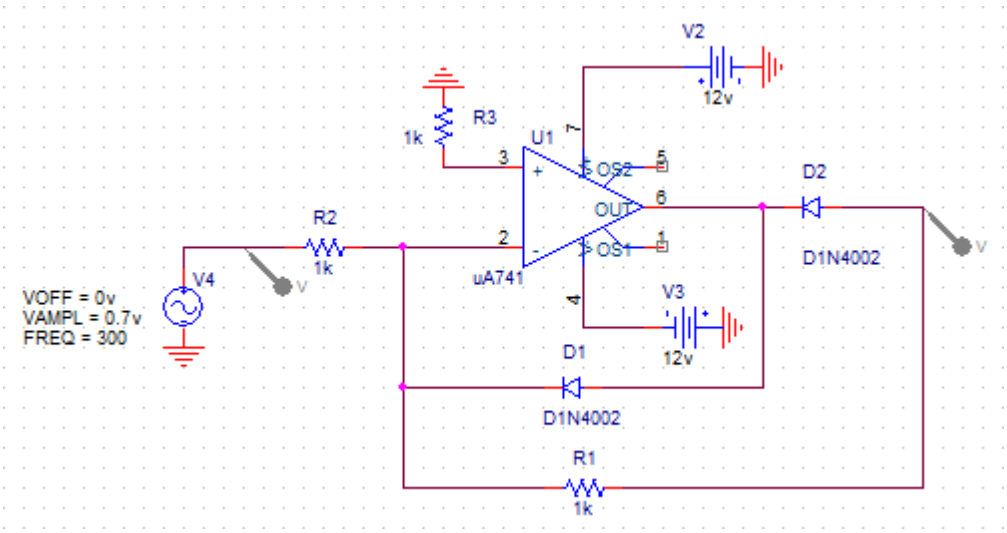
Frequency Response :



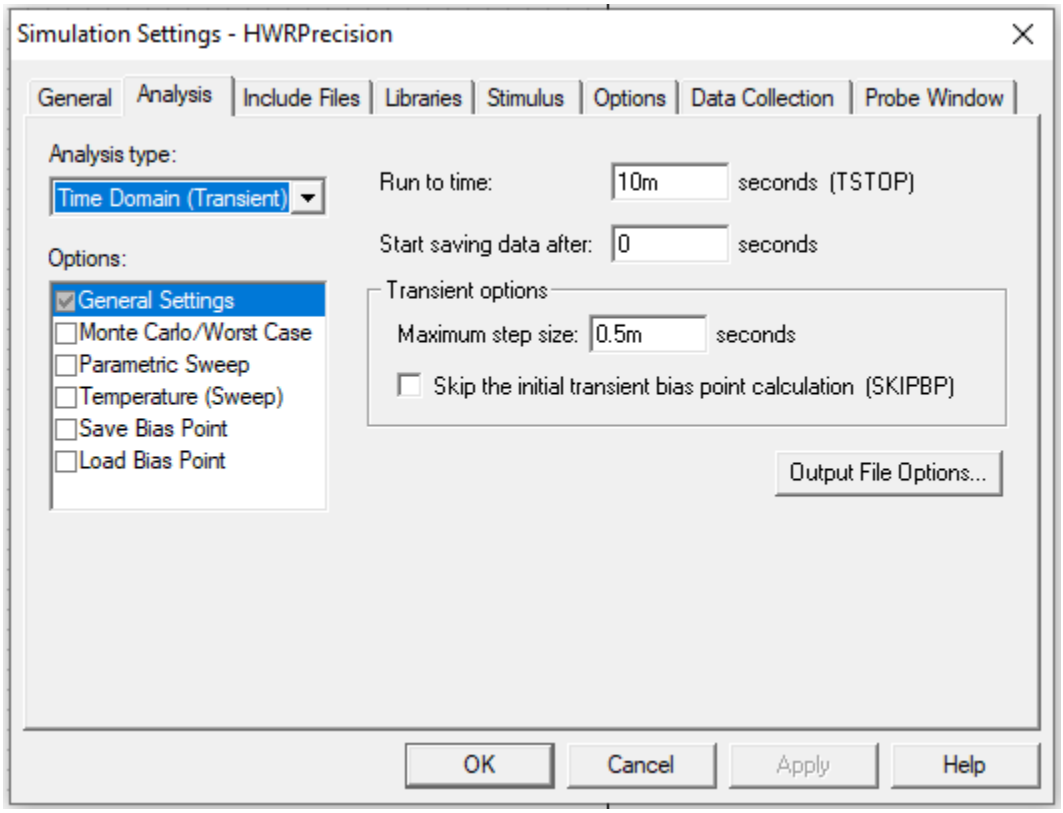
Experiment No. 11

PRECISION HALF AND FULL WAVE RECTIFIER

HALF WAVE PRECISION RECTIFIER:



Simulation Profile :



***Design*:**

$A = -R_f / R_1$

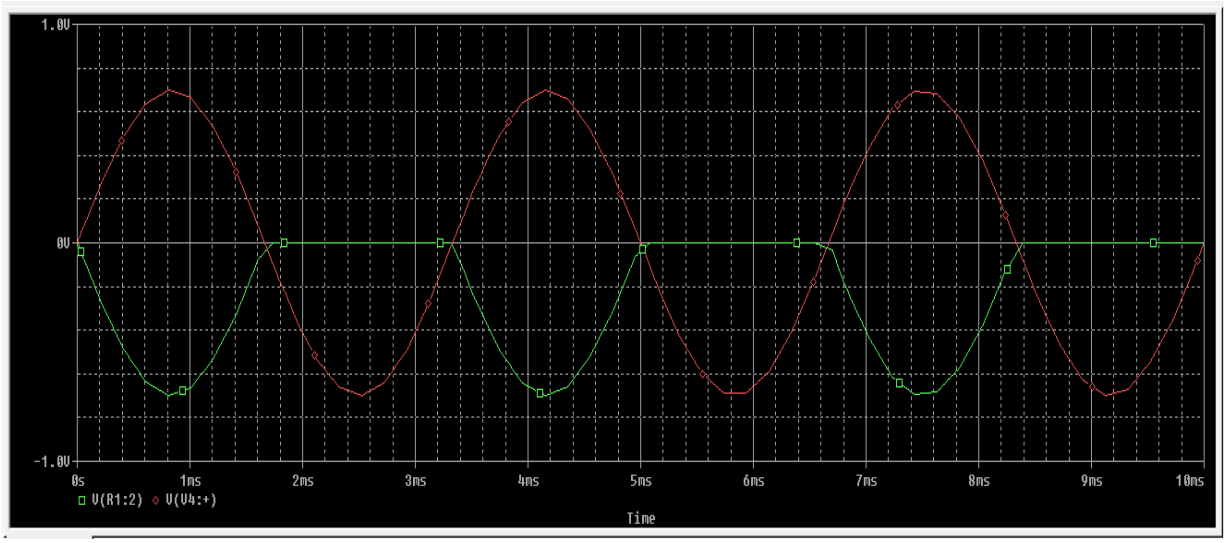
$Vo = -R_f / R_1(Vi)$

$R_f / R_1 = slope = 10$

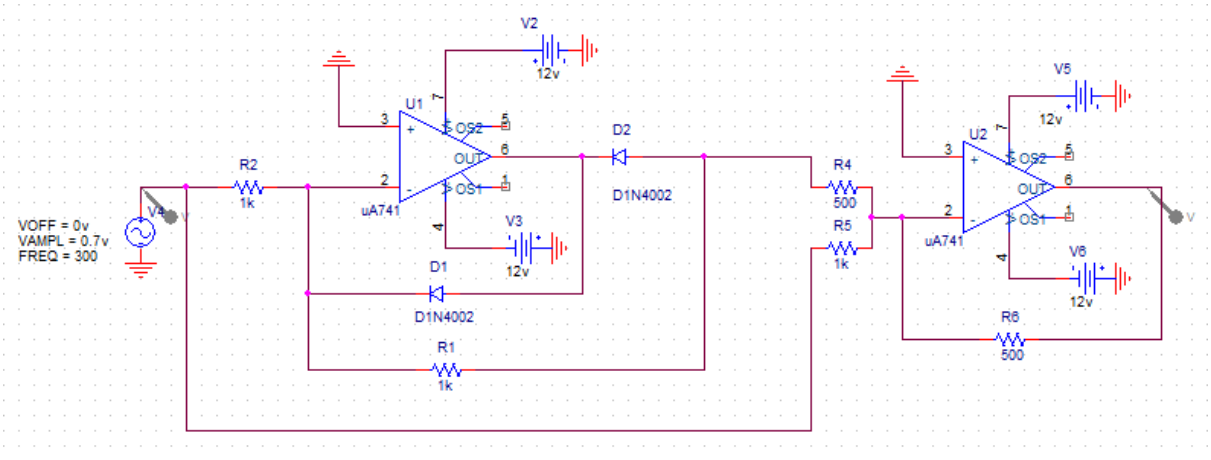
$R_f = 10\, R_1$

Let R_1=1KΩ, then R_f = 10KΩ

Waveform:



FULL WAVE PRECISION RECTIFIER:



***Design*:**

Let

R1=R2=R3=R5=1KΩ

R4=R/2=470Ω

For positive cycle, Vo = -[(R5/R3)Vi + (R5/R4)(-Vi)]

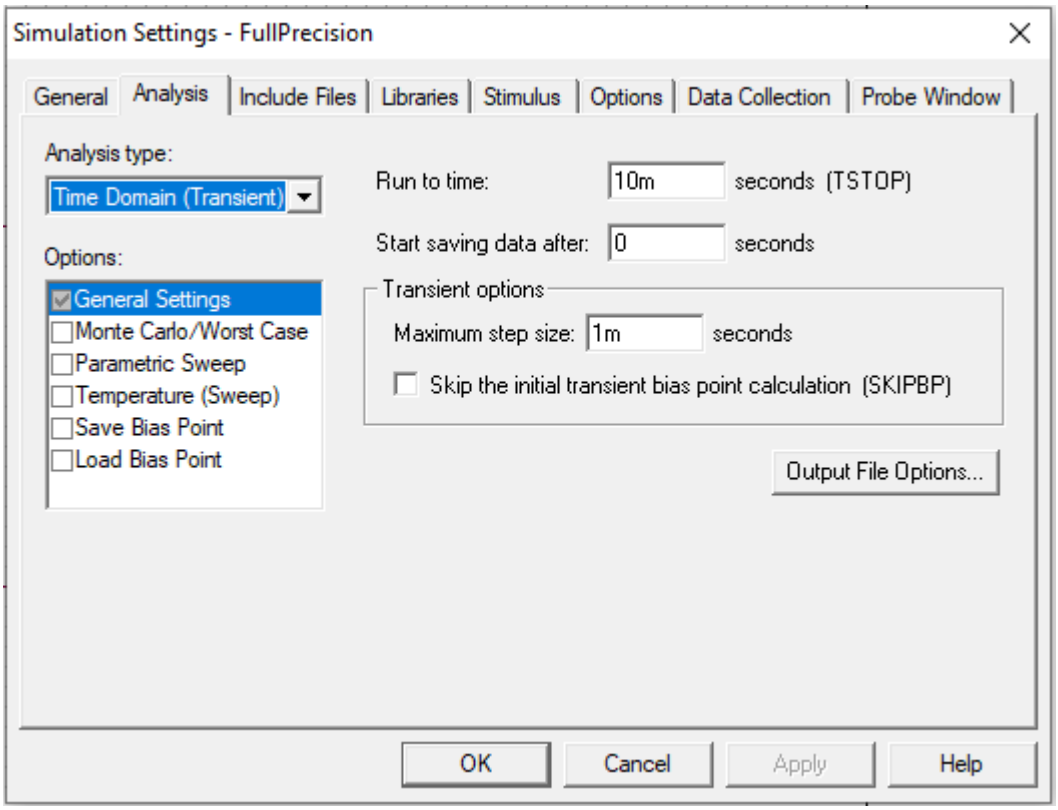
= -[(R/R)Vi + (R / (R/2))(-Vi)]

= -[Vi-2Vi] = Vi

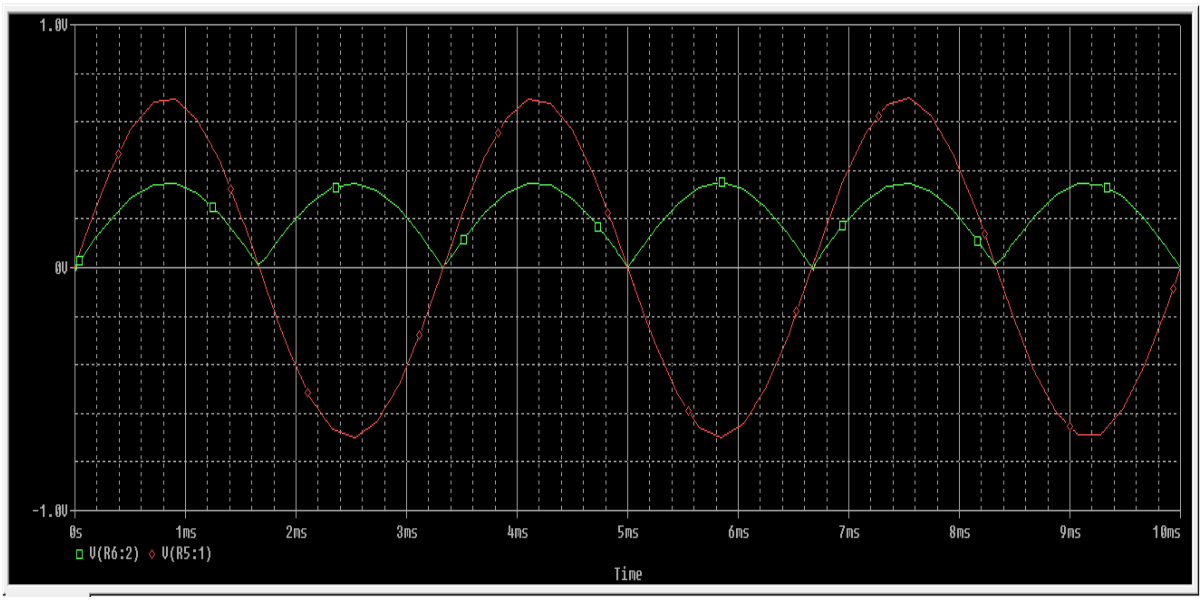
For Negative cycle, Vo = -[(R5/R3)Vi + (R5/R4)(-Vi)] = -[R/R(-Vi)]

Vo = Vi

Simulation Profile:



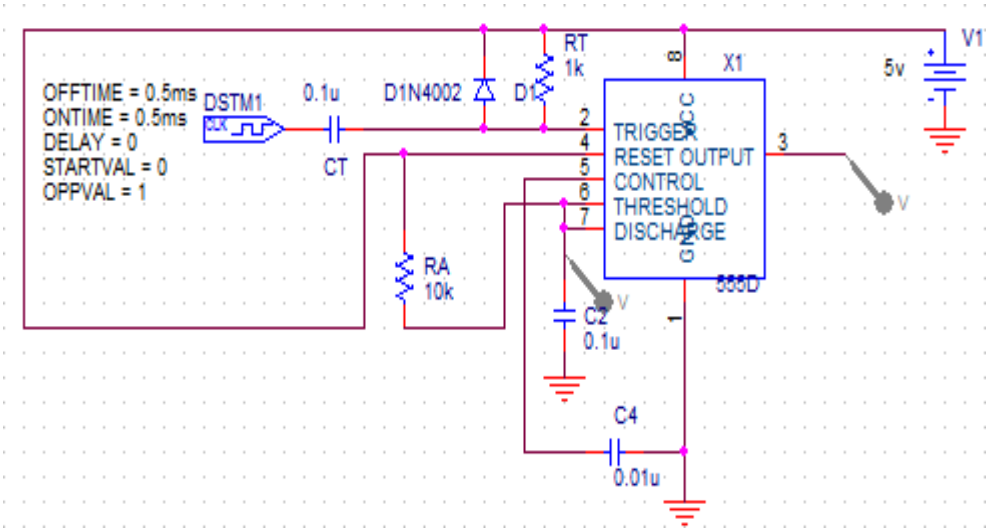
Waveform:



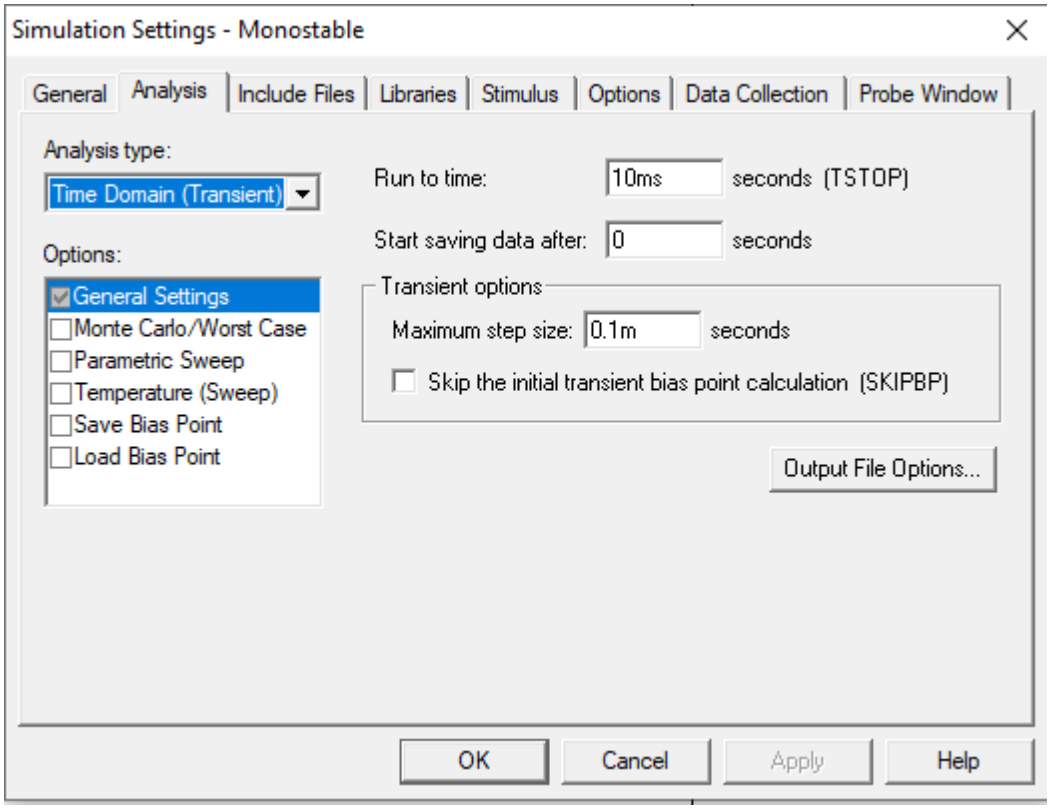
Experiment No. 12

MONOSTABLE AND ASTABLE MULTIVIBRATOR USING 555 TIMER

MONOSTABLE MULTIVIBRATOR:



Simulation Profile :



Design :

O/p pulse width = Td = 0.5msec

For Monostable multivibrator, Td= 1.1RaC Let C=0.01µF

$0.5x10^{-3} = 1.1xR_a \times 0.01x10^{-6}$

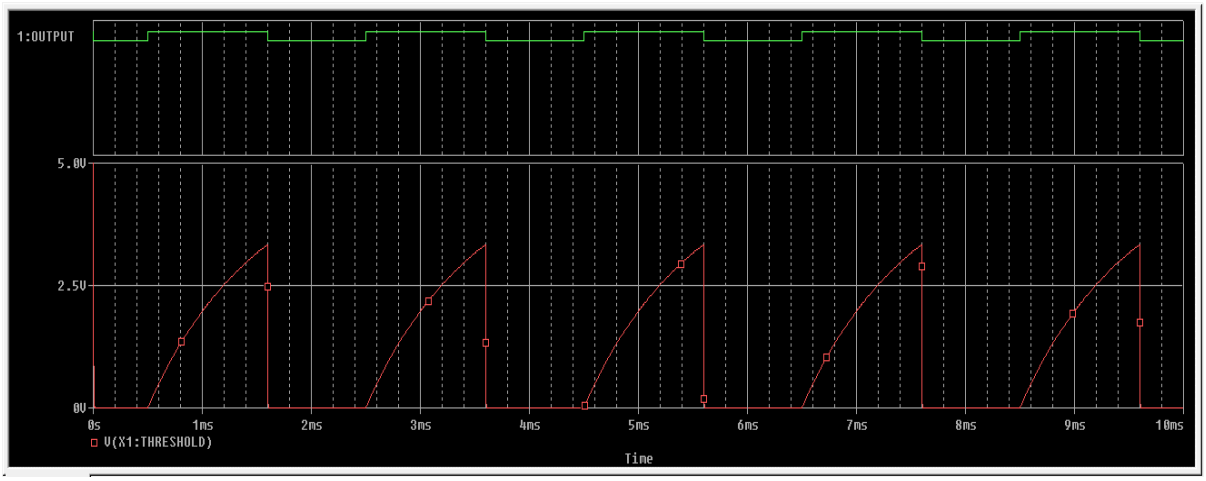
$R_a = 45.45$ KΩ , choose $R_a = 47$KΩ Vut ,upper threshold Vg = 2/3 Vcc Let f = 1KHz, then T = 1mSec R_TC_T <<T

$R_TC_T = 0.1T$, Assume $C_T = 0.01\mu F$ $R_T = 0.1x1x10^{-3}/0.01x10^{-6} = 1K\Omega$

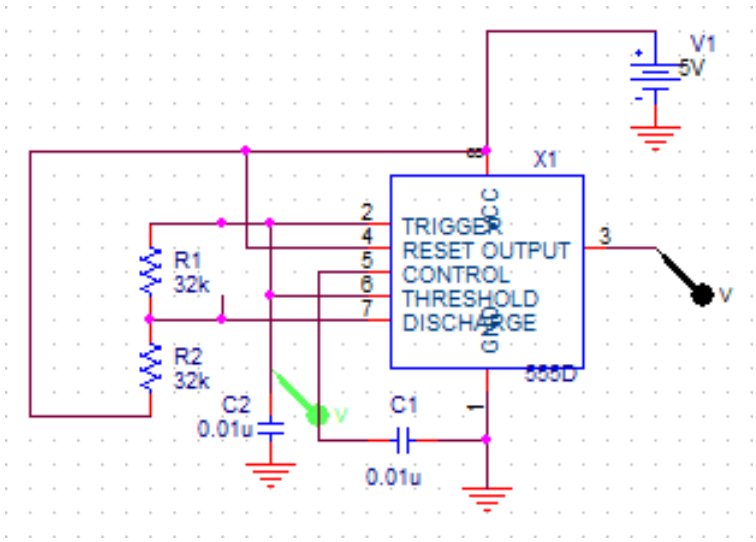
Duty cycle: D = (Td/T) x 100%

$D = (0.5x10^{-3}/1x10^{-3})x\ 100\% = 50\%$

Waveform:



ASTABLE MULTIVIBRATOR:



Design:

For Duty cycle 60%

Charging time T1=0.693*(Ra+Rb)*C Discharging time T2=0.693*Rb*C

Let f=1 kHz and choose duty cycle = 60% Duty cycle D = T1/T where T = 1/f = 1mSec T1 =

D x T = 60% x $1x10^{-3}$ = $0.6x10^{-3}$Sec

T = T1 + T2

T2 = T - T1 = $1x10^{-3}$ – $0.6x10^{-3}$ = $0.4x10^{-3}$ Sec T2 = 0.693 x Rb x C

Assume C = 0.1μF Rb = T2/(0.693xC)

= 0.4x10-3/(0.693x0.1x10-6) = 5.7KΩ

T1=0.693x(Ra+Rb)xC

(Ra + Rb) = T1/(0.693xC)

Ra = [0.6x10-3/ (0.693x0.1x10-6)] – 5.7x103

Ra = 2.95KΩ, choose Ra = 3K Ω

Note: T1 = Ton and T2 = Toff

For Duty cycle 50%

Charging time T1=0.693*Ra*C Discharging time T2=0.693*Rb*C

Let f=1 kHz and choose duty cycle = 50% Duty cycle D = T1/T

where T = 1/f = 1mSec

T1 = D x T = 50% x $1x10^{-3}$ = $0.5x10^{-3}$Sec T = T1 + T2

T2 = T - T1 = $1x10^{-3}$ – $0.5x10^{-3}$

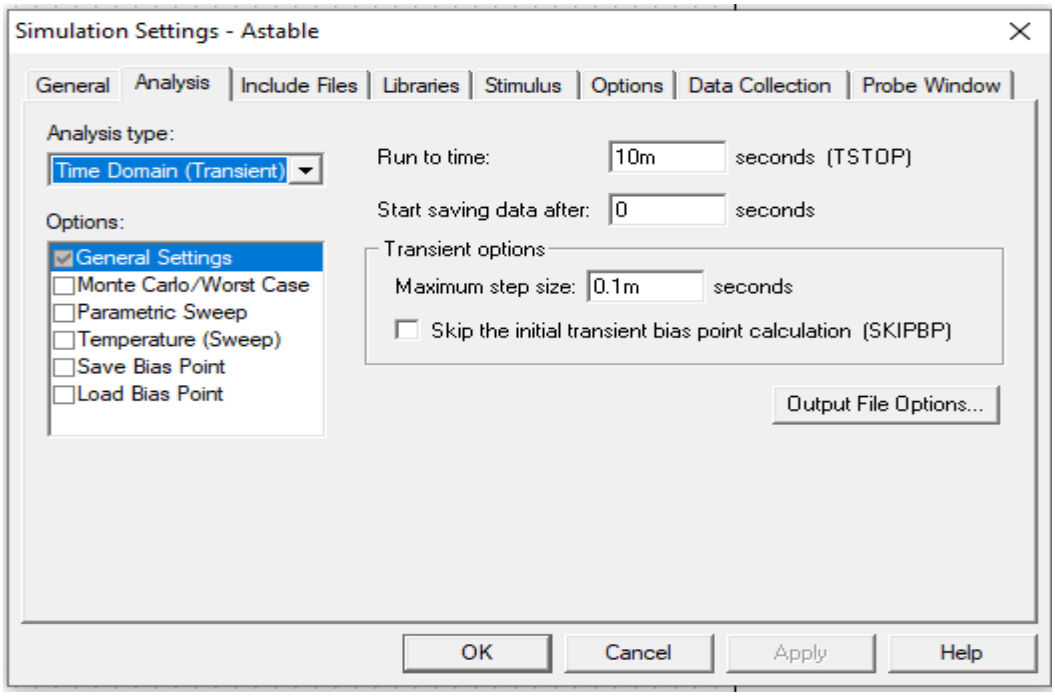
Therefore, T2 = $0.5x10^{-3}$ Sec T2 = 0.693 x Rb x C

Assume C = 0.1μF Rb = T2/(0.693xC)

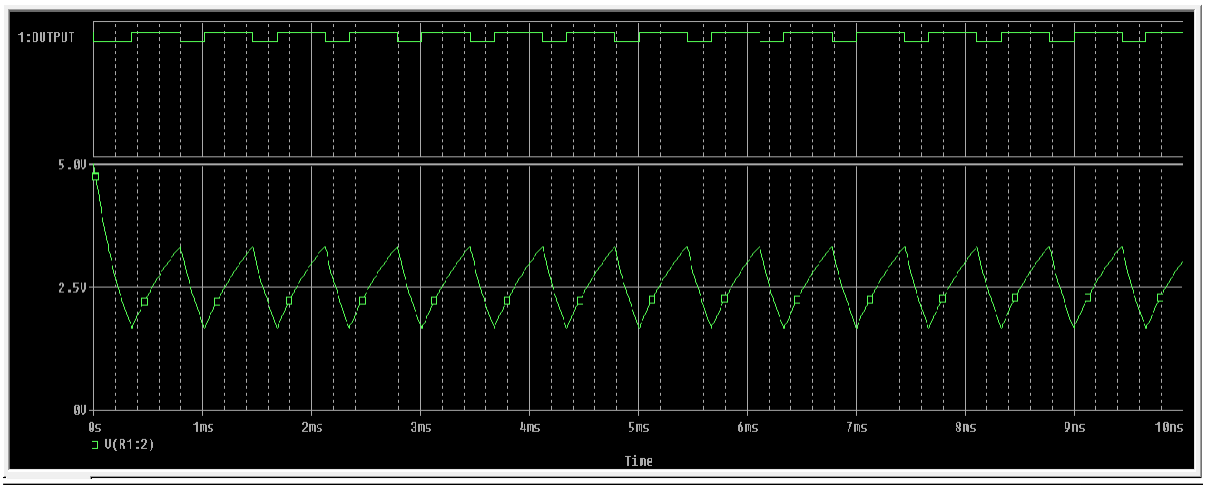
= 0.5x10-3/(0.693x0.1x10-6) = 7.2KΩ

T1=0.693 x Ra x C Ra = T1/(0.693xC)

Ra = 0.5x10-3/ (0.693x0.1x10-6) Ra = 7.2KΩ

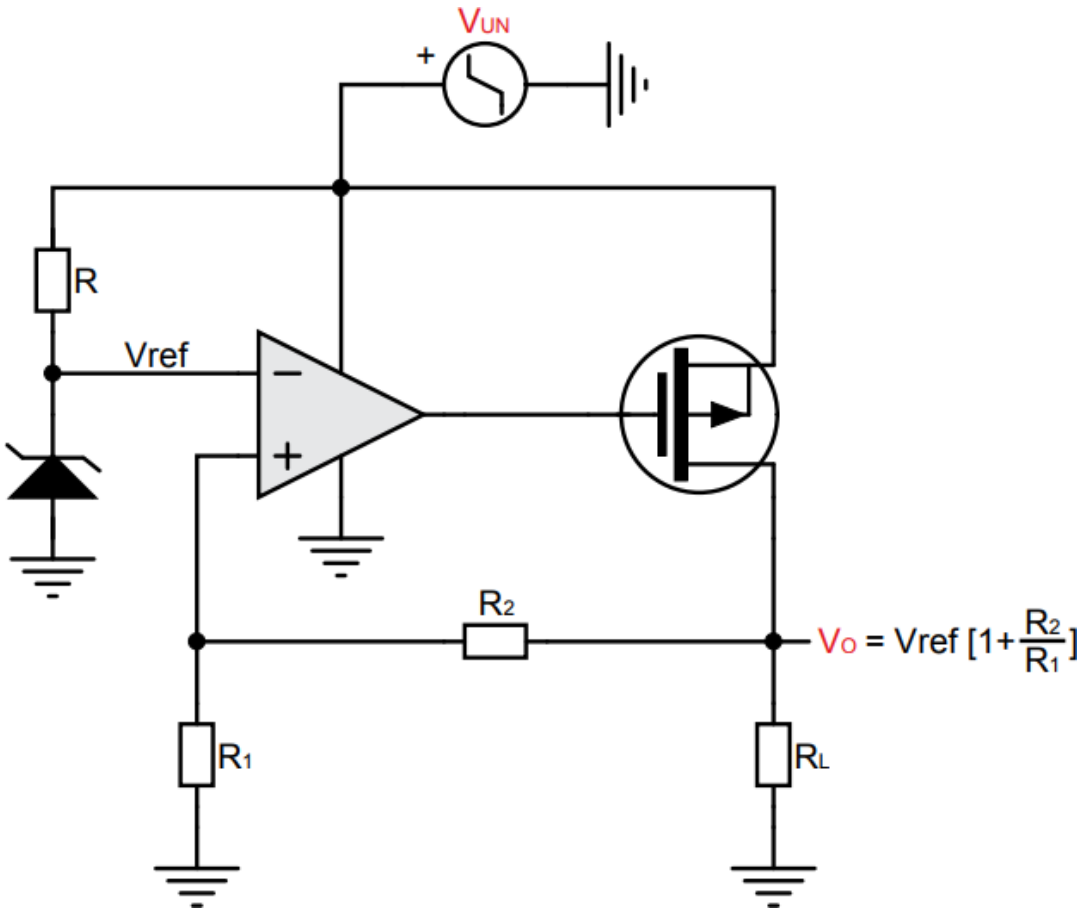

Simulation Settings - Astable
General
Analysis
Include Files
Libraries
Stimulus
Options
Data Collection
Probe Window
Analysis type:
Time Domain (Transient)
Options:
General Settings
Monte Carlo/Worst Case
Parametric Sweep
Temperature (Sweep)
Save Bias Point
Load Bias Point
Run to time:
10m
seconds (TSTOP)
Start saving data after:
0
seconds
Transient options
Maximum step size:
0.1m
seconds
Skip the initial transient bias point calculation (SKIPBP)
Output File Options...
OK
Cancel
Apply
Help

Waveform:


1:OUTPUT
5.0V
2.5V
0V
0s
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
V(R1:2)
Time

Circuit Diagram-A:

Low Dropout (LDO) regulator



Mini project

Low Dropout (LDO) regulator

Aim: Generate 3V output when input voltage is varying from 4V to 5V.

Apparatus:

Sl. No.	Particulars	Range	Quantity
1.	uA741		1
2.	Resistor	100KΩ	1
3.	Buzzer	6-12V	1
4.	Connecting wires	-	1 set

Procedure:

1. Rig up the circuit as shown in the circuit diagram-A.
2. Apply +5V supply to VCC (pin no 8).
3. Keep the probes/wires inside the water container.
4. Observe the output.

Theory:

LDO is used to produce regulated voltage for high efficiency low noise applications. In case of DC-DC converter switching takes place and switching is a source of noise but in LDO no switching takes place hence it is used as voltage regulator in low noise high efficient systems. LDO uses PMOS along with OP-Amp so that power dissipation in OP-Amp is minimal and efficiency is high. The regulated output voltage is given by

Result:

Question Bank

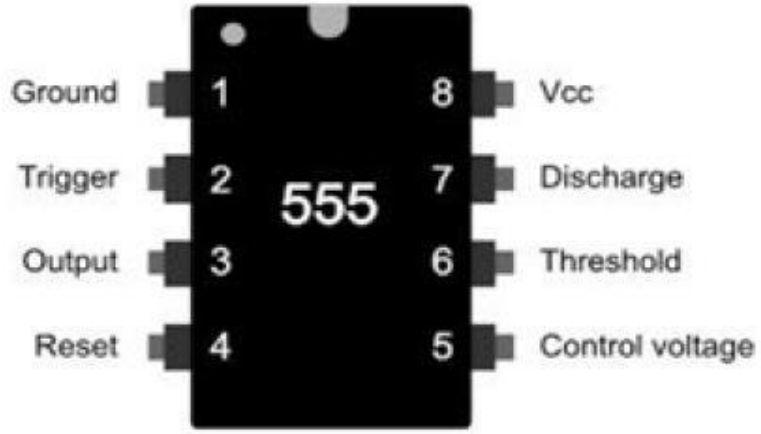
1. a) Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.
   b) Using PSpiece simulate RC phase shift oscillator.
2. a) Design and set up the BJT common emitter voltage amplifier without feedback and determine the gain- bandwidth product, input and output impedances.
   b) Using PSpiece simulate Hartley oscillator.
3. a) Design and set up the BJT common emitter voltage amplifier with feedback and determine the gain- bandwidth product, input and output impedances.
   b) Using PSpiece Simulate the frequency response of a Narrow Band-pass Filter.
4. a) Design and set-up BJT Colpitts Oscillator
   b) Using PSpiece Simulate the frequency response of a Narrow Band-reject Filter.
5. a) Design and set-up BJT Crystal Oscillator
   b) Using PSpiece simulate Precision Half wave rectifier.
6. a) Design active second order Butterworth low pass filter.
   b) Using PSpiece simulate Precision Full wave rectifier.
7. a) Design active second order Butterworth high pass filter.
   b) Using PSpiece simulate Monostable Multivibrator using 555 Timer.
8. a) Design Adder circuit using Op-Amp.
   b) Using PSpiece simulate Astable Multivibrator using 555 Timer.
9. a) Design an Integrator circuit using Op-Amp.
   b) Using PSpiece simulate RC phase shift oscillator.
10. a) Design a Diffrentiator circuit using Op-Amp.
    b) Using PSpiece simulate Hartley oscillator.
11. a) Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.
    b) Using PSpiece Simulate the frequency response of a Narrow Band-pass Filter.
12. a) Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
    b) Using PSpiece Simulate the frequency response of a Narrow Band-reject Filter.
13. a) Design Monostable Multivibrator using 555 Timer.
    b) Using PSpiece simulate a Precision Half wave rectifier.
14. a) Design Astable Multivibrator using 555 Timer.
    b) Using PSpiece simulate a Precision Full wave rectifier.

VIVA QUESTIONS

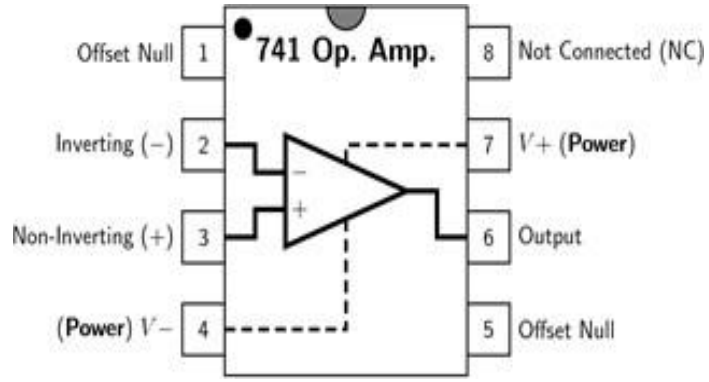
1. What is Op-amp? What are the ideal characteristics of opamp.
2. Give the practical values of voltage gain, Z_{in}, Z_{out} of anop-amp.
3. What is meant by CMRR? What is its significance.
4. Why gain of op-amp should be infinite.
5. What is slew rate, output offset voltage.
6. What is meant by maximum output voltage swing.
7. What is meant by inverting amplifier.
8. What is meant by non-inverting amplifier.
9. What is a voltage follower? How do you realize a voltage follower.
10. What is a comparator?
11. Why the output of comparator is always square wave.
12. Which circuit is called regenerative comparator and why.
13. What is trip point in comparator?
14. What are the limitations of comparator?
15. What is the condition for the circuit to work as integrator and differentiator.
16. What is ZCD and give one of its applications?
17. What is summer.
18. What is Schmitt Trigger.
19. Explain the working of Schmitt trigger.
20. What is meant by UTP and LTP.
21. Define Dead band or Dead zone.
22. Mention the applications of Schmitt Trigger.
23. Define Rectifier.
24. Name the types of Rectifier.
25. What is Precision Rectifier.
26. Realize the rectifier circuits using diodes.
27. Mention types of precision rectifier.
28. Explain the working of Full Wave Precision Rectifier.
29. Define Conversion.
30. Different types of D/A Converter.
31. Working of R-2R D/A Converter.
32. What do you understand by DAC and ADC? Where is it used.
33. What is advantage of R-2R DAC over other type DAC.

34. What is resolution (step size) in a DAC.
35. What is offset error in a DAC.
36. What are the different types of ADC.
37. Which is the fastest ADC? What are its limitations.
38. Which is the most commonly used ADC.
39. What is a filter.
40. Distinguish between active and passive filters.
41. Distinguish between analog and digital filters.
42. What are the advantages of active filters over passive filters.
43. Explain the classification of filters.
44. Define low pass filter.
45. Define high pass filter.
46. Why inductors are not often used in filters.
47. What are the applications of filters.
48. Describe amplitude modulation.
49. Describe frequency modulation.
50. Define modulation index.
51. What is percentage modulation.
52. What is pre-emphasis ? why it is used.
53. What is De-emphasis ? why it is used.
54. Explain the working envelope detector.
55. Compare various types of frequency demodulators.
56. Define low level and high level modulation.
57. What is noise? Noise is difficult to eliminate but its effect can be minimized, justify.
58. Define figure of merit.
59. Explain the operation of slope detector circuit.
60. Define over modulation.
61. Explain Pulse amplitude modulation.
62. Explain pulse width modulation.
63. Compare PAM with PWM.
64. Explain pulse position modulation.
65. What are the advantages of PPM over PAM.

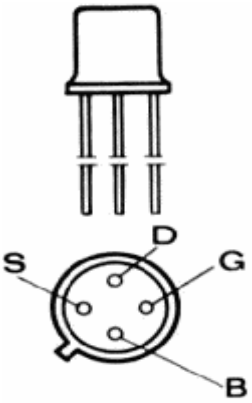
PIN CONFIGURATIONS

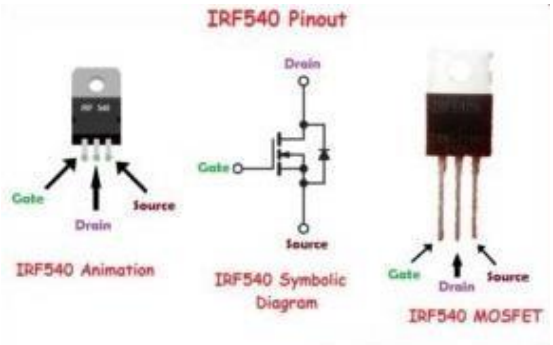


555 timer pin diagram



Op-Amp µA741 pin diagram





JFET BFW10 Pin out **MOSFET IRF540N Pin out**

-------END-------