Digital VLSI Design			
Course Code	22LEL12	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours Theory and 10 -12 Practical Sessions	Total Marks	100
Credits	04	Exam Hours	04

Course Learning Objectives:

- To understand the operation of MOS transistor, Scaling and Small Geometry Effects.
- To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter.
- To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits.
- To know Chip Input and Output Circuits, Clock Generation and Distribution Circuits, Design for Manufacturability.

Module-1

MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.

Teaching-Learning Process	Chalk and Talk, Power Point Presentations.

Module-2

MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load,CMOS Inverter.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4

Semiconductor Memories: Introduction, Dynamic Random-Access Memory (DRAM), Static Random-Access Memory (SRAM).

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-5

BiCMOS Logic Circuits: Introduction, BiCMOS Applications.
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

PracticalComponentofIPCC:ConducttheexperimentsusingCadence/ Mentor Graphics /Xilinx ISE System Edition 14.7/XUP SPARTAN 3E Kit with USB Programming cable

Sl. No.	Experiments
1	To plot the (i) output characteristics & (ii) transfer characteristics of an n-channel and p-channel MOSFET.
2	To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.
3	To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.
4	To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.
5	To design and plot the characteristics of a positive and negative latch based on multiplexers.
6	To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers
7	To Design D, T, JK Flip Flops
8	To Design BCD adder

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1. Two Tests each of **20 Marks**

2. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE) .

Suggested Learning Resources:

Books

1. "Sung Mo Kang & Yusuf Leblebici", CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition.
2. "Neil Weste and K. Eshraghian", Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000.
3. "Wayne, Wolf", Modern VLSI Design: System on Silicon, Prentice Hall PTR/ Pearson Education Second Edition, 1998

4. "Douglas A Pucknell& Kamran Eshraghian", Basic VLSI Design PHI 3rd Edition

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=57uTCtSQV50&list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS
2. https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.	L4
CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	L4
CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	L3
CO4	Interpret critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	L2
CO5	Use Bipolar and Bi-CMOS circuits in very high-speed design.	L3

Advanced Embedded System			
Course Code	22LEL13	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 slots for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning Objectives:

- To understand the concepts of embedded system design.
- To learn real design challenges of the system under development.
- To gain the essential knowledge required to design practical real-time embedded systems and appropriate real-time operating system (RTOS) product to be used.
- To know networking aspects of the embedded systems and Hardware-Software Co-design.

Module-1

Introduction of Embedded System: Embedded System: Embedded vs General computing system, classification, application and purpose of ES.

Typical of Embedded System: Communication Interface

The Strategy: Definition, Common Characteristics, Some Quality Metrics in ES Design, Versatility Factors for ES Product, Technologies Involved (Processors, Platforms, Devices-IC Technology), Hardware/Software Co-design

Use Cases: What Are Use Cases, Casual Versus Structured Version, Black Box Versus White Box, Hub and Spoke Model, Details of the Use Case Model Entities (Actor, Stakeholder, Primary Actor, Supporting Actor, Scope, Scenarios, Levels, Use Case Entities and Their Relation, When Are We Done, Standard Use Case Template)

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Models and Architectures: Representation of a Design, Model Taxonomy, Finite-State Machine (Mealy) Model, Petri Nets, Hierarchical Concurrent FSMs, Activity-Oriented Data Flow Graphs, Control Flow Graphs (Flowchart), Structure-Oriented Models, Data-Oriented Entity-Relationship Model, Jackson's Structured Programming Model, Heterogeneous Models

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Specification Languages: SystemC: Characteristics of ESL for Embedded Systems, System C, Processes.

UML for Embedded Systems: Motivation, Typical Tasks and Roles in System Engineering, UML Diagrams, Structural Diagrams, Behavioural Diagrams

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Real-Time Systems: Definition and Examples, Broad Classification of RTS, Terms in RT Systems, Periodic Schedule, Precedence Constraints and Dependencies, Scheduling Algorithms–Classification, Clock-Driven Scheduling, Priority-Driven Periodic Tasks, Dynamic Priority Algorithms, Scheduling Sporadic Jobs, Resource Access and Contention.

Real-Time Operating Systems (RTOS): Introduction, RTOS Concepts, Basic Design Using RTOS Case Study 1, Concept-Process and Threads.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Real-Time Operating Systems (RTOS): Posix, pThreads, Thread Synchronization, Design Strategies

Networked Embedded Systems (NES): Introduction, Characteristics, Broad Segments of NES, Automotive NES, CAN (Controller Area Network).

HW-SW Co-design: Introduction, Factors Driving Co-design, Co-design Problems, Conventional Model for HW-SW Design Process, Integrated Co-design Process, System Partitioning, Partitioning Algorithms.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be

deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1. (Transactions on computer systems and networks) k. c. s. murti - design principles for embedded systems-springer (2022)
2. Introduction to embedded systems K. V. Shibu TMH education Pvt. Ltd. 2009
3. Embedded systems - A contemporary design tool James K. Peckol John Wiley 2008
4. The Definitive Guide to the ARM Cortex-M3 Joseph YiuNewnes, (Elsevier) 2 ndedn, 2010.

Web links and Video Lectures (e-Resources):

1. https://youtu.be/GaZBpY9Ys1Y
2. https://youtu.be/SUusup7FfJo
3. https://youtu.be/dHsHP9RrXBw?list=PLJ5C_6qdAvBH-JNRIlupFb44miyx9M8JD
4. https://youtu.be/vn7aT9-cYzQ
5. https://youtu.be/-rWGzFDLnAY

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Design and Develop Embedded Systems with hardware software co-design.	L3
CO2	Analyze different models and architecture of the Embedded Systems and Networked Embedded Systems	L4
CO3	Verify the performance of RTS and RTOS	L3, L4

Digital Circuits and Logic Design			
Course Code	22LEL14	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 hours Theory + 10-12 slots for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- Understand the concepts of sequential machines.
- Design Sequential Machines/Circuits.
- Analyze the faults in the design of circuits.
- Apply fault detection experiments to sequential circuits.
- Comprehend the structure of sequential machines

Module-1

Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Fault-Location Experiments, Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbook:

'Switching and Finite Automata Theory', ZviKohavi, TMH,ISBN: 978_0_07_099387_7, 2ndEdition, 2008.

Reference Books:

1. 'Digital Circuits and logic Design', Charles Roth Jr., Cengage Learning, 7thedition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design', Parag K Lala, Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. 'Theory of computer science – Automata, Languages and Computation', Mishra & Chandrasekaran, 2ndEdition, PHI, 2004.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the concepts of sequential machines.	L2
CO2	Design Sequential Machines/Circuits.	L3
CO3	Analyze the faults in the design of circuits.	L4
CO4	Apply fault detection experiments to sequential circuits.	L3
CO5	Understand the structure of sequential machines.	L2

WIRELESS SENSOR NETWORKS			
Course Code	22LEL15	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: Thiscoursewillenablestudentsto:

- Learn the basic concepts of Wireless sensor networks architecture and protocols.
- Understand the challenges in designing a Wireless sensor network.
- Understand the function of Data link and Network layer Protocols.
- Understand the function of Transport layer Protocols.
- Analyze wireless sensor network system for different applications under consideration

Module-1

INTRODUCTION: Sensor Mote Platforms, WSN Architecture and Protocol Stack.
WSN Applications: Military Applications, Environmental Applications, Health Applications, Home Applications, Industrial Applications.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

FACTORS INFLUENCING WSN DESIGN: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption.
Physical Layer: Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

MEDIUM ACCESS CONTROL: Challenges for MAC, CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, Hybrid Medium Access.
Network Layer: Challenges for Routing, Data-centric and Flat Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Transport Layer: Challenges for Transport Layer, Reliable Multi Segment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol, Event-to-Sink Reliable Transport (ESRT) Protocol, GARUDA
Application Layer: Source Coding (Data Compression), Query Processing, Network Management.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

SPREAD SPECTRUM SIGNALS FOR DIGITAL COMMUNICATION: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spreadspectrum signals, Time hopping SS, Synchronization of SS systems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the Cos and Pos

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Wireless Sensor Networks', Ian F. Akyildiz and Mehmet Can Vuran, JohnWiley&SonsLtd.ISBN 978-0-470-03601-3(H/B),2010
2. 'Wireless Sensor Networks: Signal Processing and Communications Perspectives', Ananthram Swami, et. Al., John Wiley & Sons Ltd., ISBN978-0-470-03557-3,2007.

Massive Open Online Courses:

https://archive.nptel.ac.in/courses/106/105/106105160/#-**Wireless** Ad Hoc and **Sensor Networks** -BY Prof. SUDIP MISHRA,IITKGP

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand challenges and technologies for wireless networks	L2
CO2	Understand architecture and sensors	L2
CO3	Describe the communication, energy efficiency, computing, storage and transmission	L4
CO4	Establishing infrastructure and simulations	L4
CO5	Explain the concept of programming in the WSN environment	L3

EmbeddedSystemsLab			
Course Code	22LELL17	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	1:2:0	SEE Marks	50
Total Hours of Pedagogy	13 Hours of teaching and 10-13 Practical sessions	Total Marks	100
Credits	2	Exam Hours	03

PartA: EDA Using Cadence OrCAD or OrCAD Lite or any EDA Tool,designandverifythefollowing:

Sl. No.	Experiments
1	3½DigitDigitalVoltmeter
2	MonolithicfunctionGenerator
3	RegulatedPowersupplies
4	BatchcounterusingTTLICs
5	DACand ADC
6	P,PI,PIDand ON/OFFControllers
7	ProgrammableTimers
8	FiltersandResonanceCircuits

PART-B:ARM-CORTEXM3 [Programming to be done using Keil uVision 4 and download theprogram on to M3 evaluationboardsuchas NXPLPC1768or ATMELATSAM3U]

Sl. No.	Experiments
1	WriteanAssemblylanguage programto calculate10+9+8+…..+1
2	WriteanAssemblylanguageprogramtolinkMultipleobjectfilesand linkthemtogether.
3	WriteanAssemblylanguage programtostoredatain RAM.
4	WriteaCprogramtoOutputthe"HelloWorld"messageusingUART.
5	WriteaCprogramtoDesignaStopwatchusinginterrupts.
6	WriteanExceptionvectortableinC
7	WriteanAssemblyLanguageProgramforlockingaMutex.
8	Write a SVC handler in C. Use the wrapper codeto extract thecorrect stack frame starting location. The C handler can then use thistoextractthestackedPClocationand thestacked register values.

Courseoutcomes:

Attheend ofthecoursethestudentwillbeableto:

1. Understandthecomputeraideddesigntoolsfortheelectroniccircuitdesigns.
2. Designandverifyanalogcircuitssuchas ADC,DAC,Controllers,etc.usingsimulationtools
3. Createandverifydigitalsystemsusing CadenceOrCAD,OrCADLiteoranyEDAtool.
4. Developassemblyprogramsfordifferentapplicationsusing ARMCortexM3 andKeil uVision-4tool.
5. DevelopCProgramsfordifferentapplicationsusingARM-CortexM3andKeiluVision-4tool.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the

journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} week of the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

BOS Recommended ONLINE Courses

Sl. No.	Course code	Course Title	National Coordinator	Instructor
1	22AUD18/ 22AEC18	Design Thinking - A Primer(4 Weeks)	NPTEL	Prof. Ashwin Mahalingam, Prof. BalaRamadurai IIT Madras
2		Computer Networks and Internet Protocol (12 Weeks)	NPTEL	Prof. Soumya Kanti Ghosh & Prof. Sandip ChakrabortyIITKGP
3		Advanced IOT Applications(8 Weeks)	NPTEL	Prof. T V PrabhakarIISc
4		Spread Spectrum Communications and Jamming(12 Weeks)	NPTEL	Prof. Debarati SenIITKGP
5		Optical Wireless Communications for Beyond 5G Networks and IoT (12 Weeks)	NPTEL	Prof. Anand SrivastavaIIITD
6		Employment Communication A Lab based course(8 Weeks)	NPTEL	Prof. Seema SinghIIT KGP
7		Embedded System Design with ARM (8 Weeks)	NPTEL	Prof. Indranil Sengupta and Kamalika Dutta IITKGP

ASIC Design			
Course Code	22LEL21	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill development activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To learn ASIC methodologies and programmable logic cells.
- To analyse physical design flow, including partitioning, floor-planning, placement and routing.
- To gain sufficient knowledge for carrying out ASIC designs.

Module-1

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.
CMOS Logic: Data path Logic Cells: Data Path Elements, Data path Operators, Cell Compilers.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

ASIC Library Design: Logical effort: Logical area and logical efficiency, Logical paths, Multi stage cells.
Programmable ASIC Logic Cells: Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Programmable ASIC I/O Cells: Xilinx I/O Block.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Low-level Design Entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.
ASIC Construction: Physical Design, CADTools.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement., KL algorithm.
Floor planning: Goals and objectives, Measurement of delay in Floor planning.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement.
Routing: Global Routing: Goals and objectives, Global routing between blocks. Detailed Routing: Goals and objectives, Left-Edge Algorithm, Special Routing, Circuit extraction and DRC.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005.
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
3. Vikram ArkalgudChandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
4. Rakesh Chadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

Web links and Video Lectures (e-Resources):

1. https://www.youtube.com/watch?v=oZSv68esbgI
2. https://www.youtube.com/watch?v=4cPkr1VHu7Q
3. https://nptel.ac.in/courses/106105161

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort.	L1, L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L2, L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition and routing with the use of CAD algorithms.	L3
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L2, L3

Advanced Digital signal processing			
Course Code	22LEL22	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 Practical sessions	Total Marks	100
Credits	4	Exam Hours	03

Course Learning objectives: This course will enable students:

- To Know the analysis of discrete time signals.
- To study the modern digital signal processing algorithms and applications.
- To Have an in-depth knowledge of use of digital systems in real time applications
- To Apply the algorithms for wide area of recent applications.

Module-1

Introduction to Digital Signal Processing: Review of Discrete time signals and systems and frequency analysis of discrete time linear time invariant systems, implementation of discrete time systems, correlation of discrete time systems Sampling, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Multirate Digital Signal Processing: Multirate signal processing and its applications, Design of Digital filters, Design of FIR filters, Design of IIR filters, frequency transformations, Digital filter banks, two channel quadrature mirror filter banks.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Adaptive filters:Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Power Spectrum Estimation:
Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman &Tukey Methods.
Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

PracticalComponentofIPCC:ConducttheexperimentsusingMATLAB/Scilab/TMS320C5XDSPProcessors

Sl.No.	**Experiments**
1.	Generate various fundamental discrete time signals
2.	Basic operations on signals (Multiplication, Folding, Scaling).
3.	Find out the DFT & IDFT of a given sequence without using inbuilt instructions.
4.	Interpolation & decimation of a given sequence.
5.	Generation of DTMF (Dual Tone Multiple Frequency) signals
6.	Estimate the PSD of a noisy signal using periodogram and modified periodogram

7.	Estimation of PSD using different methods (Bartlett, Welch, Blackman-Tukey).
8.	Design of Chebyshev Type I, II Filters.
9.	Cascade Digital IIR Filter Realization.
10.	Parallel Realization of IIR filter.
11.	Estimation of power spectrum using parametric methods (YuleWalker&Burg).
12.	Time-Frequency Analysis with the Continuous Wavelet Transform.
13.	Signal Reconstruction from Continuous Wavelet Transform Coefficients.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

4. Two Tests each of **20 Marks**
5. Two assignments each of **10 Marks/One Skill Development Activity of 20 marks**
6. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The**15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test at the end /after completion of all the experiments shall be conducted for 50 marks and scaled down to 05 marks**.**

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

5. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
6. The question paper will have ten questions. Each question is set for 20 marks.
7. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
8. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be

included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course(CIE+SEE)

Suggested Learning Resources:

Text Books

1. Digital Signal Processing Principles, Algorithms, and Applications by John G. Proakis, Prentice-Hall International Inc., 4th Edition, 2012.
2. Theory and Application of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold.

Reference Books

1. Oppenheim, Alan V. Discrete-time signal processing. Pearson Education India, 1999.
2. Mitra, Sanjit Kumar, and YonghongKuo. Digital signal processing: a computer-based approach. Volume 2. New York: McGraw-Hill Higher Education, 2006.

Web links and Video Lectures (e-Resources):

1. https://ekeeda.com/degree-courses/electrical-engineering/advanced-digital-signal-processing
2. https://dss-kiel.de/index.php/teaching/lectures/lecture-advanced-digital-signal-processing

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Able to analyze and implement the frequency analysis & correlation of discrete-time linear time invariant systems.	L4
CO2	Able to implement sampling rate conversion by decimation & Interpolation process and design digital filter banks	L4
CO3	Able to analyze forward and backward linear prediction of a stationary random process using Levinson-Durbin Algorithm	L4
CO4	Able to understand and analyze adaptive filters and its application using LMS algorithm & RLS algorithm.	L4
CO5	Able to understand parametric & non-parametric methods for power spectrum estimation.	L2

Professional Elective -I

Nanoelectronics			
Course Code	22LEL231	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technology.
- Analyse the requirements for new materials and device structure in the future technologies.

Module-1

Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nano systems.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.
CarbonNanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.
Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Methods of measuring properties: atomic, crystallography, microscopy, spectroscopy.
Applications: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIPs, NEMS, MEMS.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. 'Nanoscale Science and Technology', Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, John Wiley, 2007

2. 'Introduction to Nanotechnology', Charles P Poole, Jr, Frank J Owens, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

1.'Hand Book of Nanoscience Engineering and Technology', Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, CRC press, 2003

Web links and Video Lectures (e-Resources):

1. https://www.digimat.in/nptel/courses/video/117108047/L01.html
2. https://archive.nptel.ac.in/courses/117/108/117108047/

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Know the principles behind Nanoscience engineering and Nanoelectronics.	L2
CO2	Apply the knowledge to prepare and characterize nanomaterials.	L3
CO3	Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials	L2
CO4	Design the process flow required to fabricate state of the art transistor technology	L3
CO5	Analyze the requirements for new materials and device structure in the future technologies.	L3

Reconfigurable Computing			
Course Code	22LEL232	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: Thiscoursewillenablestudentsto:

- Understand the fundamental principles and practices in reconfigurable architecture.
- Simulate and synthesize the reconfigurable computing architectures.
- Understand the FPGA design principles, and logic synthesis
- Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
- Design digital systems for a variety of applications on signal processing and system on chip configurations.

Module-1

Introduction: History, Reconfigurable vs Processor based system, RC Architecture.Reconfigurable Logic Devices: Field Programmable Gate Array, Coarse Grained ReconfigurableArrays.Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey ofReconfigurable Computing System.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Implementation: Integration, FPGA Design flow, Logic Synthesis. High Level Synthesis for Reconfigurable Devices**:** Modelling, Temporal Partitioning Algorithms.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

3. Three Unit Tests each of **20 Marks**
4. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

6. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
7. The question paper will have ten full questions carrying equal marks.
8. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
9. Each full question will have a sub-question covering all the topics under a module.
10. The students will have to answer five full questions, selecting one full question from each module

.

Suggested Learning Resources:

Text Books

1. Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays by M. Gokhale and P. Graham,Springer, ISBN: 978-0-387-26105-8, 2005.
2. Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications by C. Bobda,Springer, ISBN: 978-1-4020-6088-5, 2007.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the new paradigm of Computing which offers flexibility, scalability and performance.	L2
CO2	Understand the notion of system/circuit redesign on the fly using dynamic reconfiguration. T	L2
CO3	Able to optimize the given system specific to underlying reconfigurable hardware.	L3
CO4	Able to bring the notion of evolvable circuit on Reconfigurable hardware.	L3
CO5	Designing a reconfigurable computing and how to utilize them for solving challenging computational problems.	L3

Cryptography and Network Security			
Course Code	22LEL233	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	

Course Learning objectives:

- Study the network security model, security attacks, mechanisms and services and to demonstrate use of various symmetric key ciphers and their principles.
- Understand the concept of Modular Arithmetic and its application in public key cryptography and apply the knowledge to solve security related problems.
- Understand the design principles of Public key cryptosystems for encryption, key exchange and authentication.
- Comprehend the concept of secured electronic transaction with web security considerations.
- Study the security threats to networks and their counter measures.

Module-1

Security services, mechanisms and attacks, OSI security model, symmetric key cryptography,substitution techniques: playfair and transposition techniques, SDES: encryption, decryptionand key generation, DES: design principles, AES: encryption and decryption model,steganography.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-2

Galois fields, extended Euclid's theorem, discrete log problem, Chinese remainder theorem,elliptic curve arithmetic, principles of public key cryptosystems.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-3

Principles of public-key cryptosystems: public-key cryptosystems, applications for public-key cryptosystems, requirements for public-key cryptography, public-key cryptanalysis, the RSA: description of the algorithm, computational aspects, the security of RSA algorithm, Diffie Hellman key exchange, cryptographic hash functions: applications of cryptographic hash functions, two simple hash functions, requirements and security, hash functions based on cipher block chaining, secure hash algorithm (SHA).

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-4

Web security considerations: web security threats, web traffic security approaches, secure sockets layer and transport layer security: SSL architecture, SSL record protocol, change cipher spec protocol, alert protocol, handshake protocol, cryptographic computations, transport layer security, secure electronic transaction: SET overview, Dual signature, payment processing.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Module-5

Viruses and related threats: Malicious programs, the nature of viruses, types of viruses, macro viruses, e-mail viruses, worms, firewalls: Firewall characteristics, types of firewalls, firewall configurations, Trusted systems: Data access control, the concept of trusted systems, trojan horse defence.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

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Suggested Learning Resources:

Books

1. William Stallings, "Cryptography and Network security: principles and practice", 2nd Edition, Prentice Hall of India, New Delhi,2002 and onwards
2. Behrouz A. Fourouzan, “Cryptography and Network security” Tata McGraw-Hill, 2008 and onwards.
3. Atul Kahate,” Cryptography and Network security”, 2ndEdition, Tata McGraw-Hill, 2008 and onwards.
4. H. Yang et al., Security in Mobile Ad Hoc Networks: Challenges and Solution, IEEE Wireless Communications, 2004 and onwards.

Web links and Video Lectures (e-Resources):

1. https://swayam.gov.in/
2. https://nptel.ac.in/

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student’s abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Identify and describe different techniques in modern cryptography	L2
CO2	Employ the modular arithmetic fundamentals to cryptography	L4
CO3	Describe, recognize and use the principles of Public key cryptosystems forvarious applications.	L4
CO4	Recognize the use of cryptography in Data Networks	L4
CO5	Analyze the security issues related to internet and networks	L5

ADVANCED COMMUNICATION SYSTEMS			
Course Code	22LEL234	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	(2:0:2)	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: Thiscoursewillenablestudents:

- To understand the concept of low pass and Band pass signals during modulation at the Transmitter.
- To analyze the Receiver performance for various types of single carrier symbol modulations through ideal and AWGN channels.
- To apply single carrier equalizers for various modulation schemes and detection methods for defined channel models
- To understand the concepts of synchronization for carrier and symbol timing recovery at receiver.
- To understand the concepts of spread spectrum systems for communications in a Jamming, multiuser and low power intercept environment.

Module-1

Signal Representation: Low pass representation of band pass signals, Low pass representation of band pass random process.
Modulation: Representation of digitally modulated Signals, Modulation Schemes without memory (Band Limited Schemes - PAM, BPSK, QPSK, MPSK, MQAM, Power Limited Schemes – FSK, MFSK, DPSK, DQPSK), modulation schemes with memory (Basics of CPFSK and CPM – Full Treatment of MSK), Transmit PSD for Modulation Schemes.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-2

Demodulation:Vector Channel, Vector Channel +AWGN, Performance parameters, Optimum Coherent Detection for power limited and Band limited schemes, Optimal Coherent detection for schemes with memory, Optimal Non– Coherent detection for schemes without and with memory (FSK, DPSK, DQPSK), Comparison of detection schemes.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-3

Bandlimited Channels: Band limited channel characterization, signalling through band limited linear filter channels, Sinc, RC, Duobinary and Modified Duobinary signalling schemes.
Linear Equalizers: Zero forcing Equalizer, MSE and MMSE. **Non-Linear Equalizers**: Decision - feedback equalization, Predictive DFE, Performance of DFE.
Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-4

Synchronization – Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery, Performance of ML estimators. Fading – Large scale, small scale; Statistical characterization of multipath channels – Delay and Doppler spread, classification of multipath channels, Binary signalling over frequency non selective Rayleigh fading channel.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Module-5

Spread Spectrum Signals For Digital Communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spreadspectrum signals, Time hopping SS, Synchronization of SS systems.

Teaching-Learning Process	Chalk and talk method, Power Point Presentation, You tube videos, Brain storming, Activity based method, Seminar

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. 1'Digital Communications', John G. Proakis, Masoud Salehi, Pearson Education, ISBN:978-9332535893, 5th edition, 2014
2. Digital Communications: Fundamentals and Applications: Fundamentals & Applications', Bernard Sklar, Pearson Education,ISBN:9788131720929, 2nd edition, 2009
3. 'Digital Communications Systems', Simon Haykin, Wiley, ISBN:9788126542314, 1st edition, 2014

Massive Open Online Courses:

1. Modern Digital Communication Techniques-By Prof. Suvra Sekhar Das | IIT Kharagpur
2. Principles of Signal Estimation for MIMO/ OFDM Wireless Communication**-By Prof. Aditya K. Jagannatham | IIT Kanpur**

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the concept of low pass and Bandpass signals representations at the Transmitter, process of Detection and Estimation at the receiver in the presence of AWGN only.	L2
CO2	Evaluate Receiver performance for various types of single carrier symbol modulations through ideal and AWGN Non-bandlimited and bandlimited channels.	L3
CO3	Design single carrier equalizers for various symbol modulation schemes and detection methods for defined channel models, and compute parameters to meet desired rate and performance requirements.	L4
CO4	Explain the concepts of multi-channel signaling scheme and synchronization for carrier and symbol timing recovery at receiver.	L2
CO5	Design and Evaluate Non band limited and Non power limited spread spectrum systems for communications in a Jamming environment, multiuser situation and low power intercept environment.	L4

Optical Communication and Networking			
Course Code	22LEL235	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives: This course will enable students to:

- Understand the various optical devices and how they operate.
- Recognize and choose various components for optical networking in accordance with the established design requirements
- Acquire knowledge of the elements of data transmission, loss obstacles, and other network operating artifacts.
- Acquire knowledge of the problems associated with setting up and maintaining the optical network's access component while keeping up with current data transmission trends.
- Build a WDM network and explore the management of components and networks.

Module-1

Introduction to optical networks: Optical Networks, optical packet switching, **Propagation of signals in optical fiber:** Different losses, Nonlineareffects, Solutions.**OpticalComponents (Part-1):** Couplers,Isolators andCirculators.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Optical Components (Part-2): Multiplexers and Filters, Optical Amplifiers, detectors. **Modulation - Demodulation:** Formats, Ideal receivers,Practical direct detection receivers, Optical preamplifiers, Bit error rates, Coherent detection.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

TransmissionSystemEngineering: Systemmodel,Powerpenalty,Transmitter,Receiver,Crosstalk.
ClientLayersofopticallayer:SONET/SDH:Multiplexing,layers,Framestructure.
AsynchronousTransferMode:ATMfunctions,Adaptationlayers,QualityofService(QoS)andflowcontrol,SignalingandRouting.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

WDM networkelements: Opticallineterminals, Opticallineamplifiers,OpticalAdd/DropMultiplexers, Optical crossconnects.
WDMNetworkDesign: Costtrade-offs,LTDandRWAproblems,Routingandwavelengthassignment,Wavelengthconversion.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

ControlandManagement(Part-1): Networkmanagementfunctions,managementframework,Informationmodel,managementprotocols,Layerswithin optical layer.
ControlandManagement(Part-2): Performanceandfaultmanagement,Impactoftransparency,BERmeasurement,Opticaltrace,Alarmmanagement, Configurationmanagement, Optical Safety.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

'OpticalNetworks',RajivRamaswami,KumarN.SivarajanandGalanHSasaki,MorganKaufmanPublishers,3rdedition,2010.

ReferenceBooks:

1. 'Optical fiber communication',John M.Senior,Pearson edition,2000.
2. 'OpticalfiberCommunication',GerdKeiser,JohnWiley,NewYork,5thEdition,2017.
3. 'FiberOptic Networks', P. E.Green,PrenticeHall,1994.

Web links and Video Lectures (e-Resources):

1. https://onlinecourses.nptel.ac.in/noc20_ph07/preview
2. https://www.classcentral.com/course/swayam-optical-communications-6699

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

Attheend ofthecoursethestudent will be able to:

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Comprehend the various optical devices and their working strategies	L2
CO2	Recognize and select various optical networking components according to the prescribed design specifications	L2
CO3	Learn the aspects of data transmission, loss hindrances, and other artifacts affecting the network operation	L2
CO4	Learn the issues involved in setting up and maintaining access part of the optical network with the latest trends in the data communication	L2
CO5	Design a WDM network and study the component and network management aspects	L4

Professional Elective- 2

Error Control Coding			
Course Code	22LEL241	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 HoursofTeachingand10to12sessionsofSkillDevelopment Activities.	Total Marks	100
Credits	03	Exam Hours	03

Course Learning objectives: Thiscoursewillenablestudentsto:

- Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.

Module-1

Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem. **Introduction to algebra:** Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2m) and its properties, (Only statements of theorems without proof) Computation using Galois field GF (2m) arithmetic, Vector spaces and Matrices.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-2

Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes (SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-3

Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-4

BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic. (Primitive BCH codes over GF (q),Reed -Solomon codes.

Majority Logic decodable codes: One -step majority logic decoding, Multiple-step majority logic.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Module-5

Convolution codes: Encoding of convolutional codes: Systematic and Nonsystematic Convolutional Codes, Feedforward encoder inverse, A catastrophic encoder, Structural properties of convolutional codes: state diagram, state table, state transition table, tree diagram, trellis diagram. Viterbi algorithm, Sequential decoding: Log Likelihood Metric for Sequential Decoding.

Teaching-Learning Process	Chalk and Talk / Power Point Presentations.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Digital Communication systems', Simon Haykin, Wiley India Private. Ltd, ISBN 978-81-265-4231-4, First edition, 2014
2. 'Error control coding', Shu Lin and Daniel J. Costello. Jr, Pearson, Prentice Hall, 2nd edition, 2004

Reference Books:

1. 'Theory and practice of error control codes', Blahut. R. E, Addison Wesley, 1984
2. 'Introduction to Error control coding', Salvatore Gravano, Oxford University Press, 2007
3. 'Digital Communications - Fundamentals and Applications', Bernard Sklar, Pearson Education (Asia) Pvt. Ltd., 2nd Edition, 2001

Web links and Video Lectures (e-Resources):

1. https://www.mooc.org/
2. https://onlinecourses.nptel.ac.in/

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.	L2
CO2	Apply modern algebra and probability theory for the coding.	L3
CO3	Compare Block codes such as Linear Block Codes, Cyclic codes, etc. and Convolutional codes.	L2
CO4	Detect and correct errors for different data communication and storage systems.	L3
CO5	Analyze and implement different Block code encoders and decoders, and also convolutional encoders and decoders including soft and hard Viterbi algorithm.	L4

SoCDesign			
Course Code	22LEL242	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	3

Course Learning Objectives:

- To understand the organization and implementation of the 3- and 5-stage pipeline ARM processor cores and ARM instruction set architecture.
- To understand the needs high-level language in application development.
- To Know the issues involved in debugging systems in embedded processor cores and in the production testing of board-level systems.
- To learn different ARM integer cores, concept of memory hierarchy and management.

Module-1

ARMOrganizationandImplementation:3-stagepipelineARMorganization,5-stagepipelineARMorganization,ARMinstructionexecution,ARMimplementation,TheARMcoprocessorinterface.

The ARM Instruction Set: Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B,BL),Branch,BranchwithLinkandexchange(BX,BLX),SoftwareInterrupt(SWI).

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-2

The ARM Instruction Set (Continued) Data processinginstructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsignedbyte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transferinstructions,Swapmemoryandregisterinstructions(SWP),Statusregistertogeneralregistertransferinstructions,Generalregistertostatus registertransferinstructions,Coprocessorinstructions, Coprocessordata operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecturev5Tonly),Unusedinstruction space,Memoryfaults, ARMarchitecturevariants

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-3

Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-pointdata types, TheARMfloating-point architecture, Expressions,Conditional statements, Loops, Functions andprocedures,Useofmemory, Run-time environment.

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-4

Architectural Support for System Development: The ARM memory interface, The Advanced MicrocontrollerBusArchitecture(AMBA),The ARM reference peripheralspecification,Hardware systemprototypingtools,The ARMulator, The JTAG boundary scan test architecture,The ARM debug architecture, Embedded Trace, Signal processing support

Teaching-Learning Process	Chalk and talk / Power point presentations

Module-5

ARM ProcessorCores:ARM7TDMI,ARM8,ARM9TDMI,ARM10TDMI,Discussion,Exampleandexercises.

Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management,Examplesandexercises.

Teaching-Learning Process	Chalk and talk / Power point presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Books

1. Steve Furber "ARM System-On-Chip Architecture" Addison Wesley, 2ndedition
2. Joseph Yiu "The Definitive Guide to the ARM Cortex-M3", Newnes, (Elsevier) , 2ndedition, 2010.
3. Sudeep Pasricha and NikilDutt," On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
4. Michael Keating, Pierre Bricaud "Reuse Methodology Manual for System on Chip designs", Kluwer Academic Publishers, 2ndedition, 2008.

Web links and Video Lectures (e-Resources):

1. https://youtu.be/PRQXzjTrCJY
2. https://youtu.be/HNbeVvfFKsQ

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.	L3
CO2	Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.	L3
CO3	Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.	L2
CO4	Use integrated ARM CPU cores (including Strong ARM) that incorporate full support for memory management.	L3
CO5	Analyze the requirements of a modern operating system and use the ARM architecture to address the same	L4

Micro Electro Mechanical Systems			
Course Code	22LEL243	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To explain MEMS
- To understand the working principles of micro systems
- To analyze the scaling laws in miniaturization

Module-1

OverviewofMEMSandMicrosystems:MEMSandMicrosystem,TypicalMEMSandMicrosystemsProducts,EvolutionofMicrofabrication, MicrosystemsandMicroelectronics, MultidisciplinaryNatureofMicrosystems,Miniaturization.Applications andMarkets.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

WorkingPrinciplesofMicrosystems:Introduction,Microsensors,Microactuation,MEMSwithMicroactuators,Microaccelerom eters,Microfluidics.

EngineeringSciencefor MicrosystemsDesignandFabrication:
Introduction,AtomicStructureofMatters,IonsandIonization,MolecularTheory ofMatterandInter-molecularForces,DopingofSemiconductors,TheDiffusion Process,Plasma Physics, Electrochemistry.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overviewon Finite Element Stress Analysis.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Scaling LawsinMiniaturization:
Introduction,ScalinginGeometry,ScalinginRigid-BodyDynamics,ScalinginElectrostaticForces,ScalingofElectromagneticForces,ScalinginElectricity, Scaling inFluidMechanics, Scaling in HeatTransfer.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

OverviewofMicro-manufacturing:Introduction,BulkMicro-manufacturing,SurfaceMicromachining,TheLIGAProcess,SummaryonMicromanufacturing.

MicrosystemDesign: Introduction,Design Considerations,ProcessDesign,Mechanical Design,UsingFiniteElementMethod.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

MEMSandMicrosystems:Design,ManufactureandNanoscaleEngineering',Tai-RanHsu,JohnWiley&Sons,ISBN:978-0470-08301-7,2ndEdition,2008

ReferenceBooks:

1. 'Microand NanoFabrication:ToolsandProcesses',HansH. Gatzen,VolkerSaile,JurgLeuthold,Springer, 2015
2. 'MicroElectroMechanicalSystems(MEMS)',DilipKumarBhattacharya,BrajeshKumarKaushik,CengageLearning.

Web links and Video Lectures (e-Resources):

1. https://www.mooc.org/
2. https://onlinecourses.nptel.ac.in/

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

Attheend ofthecoursethestudent will be able to:

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Abletounderstand the MEMS and Micro systems	L1 L2
CO2	Abletounderstand and analyze the mechanics for Microsystems design	L1 L2 L3
CO3	Abletoanalyzethe scaling laws in miniaturization	L4
CO4	Simplify the design of micro devices, micro systems using the MEMS fabrication process	L4
CO5	Choose a micromachining technique, such as bulk micromachining and surface micromachining for a specific MEMS fabrication process	L3

Real Time Operating System			
Course Code	22LEL244	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives:

- To understand a typical embedded system and its constituents
- To learn the selection process of processor and memory for the embedded systems
- To learn communication buses and protocols used in the embedded and real-time systems
- To understand real-time operating system and the types of RTOS
- To learn various approaches to real-time scheduling
- To learn software development process and tools for RTOS applications

Module-1

Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Re-entrant Functions.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Processing with Real Time Scheduling: Scheduler Concepts, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, checking return codes, Single-step debugging, Test access ports, Trace Ports.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving intertask /thread communication.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1) Three Unit Tests each of **20 Marks**
2) Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1) The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2) The question paper will have ten full questions carrying equal marks.

3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4) Each full question will have a sub-question covering all the topics under a module.
5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Real-Time Embedded Systems and Components', Sam Siewert, Cengage Learning, India Edition, 2007.
2. 'Embedded/Real Time Systems, Concepts, Design and Programming, Black Book', Dr. K.V.K.K Prasad, Dream Tech Press, New edition, 2010.

Reference Books:

1. 'Real Time System', James W S Liu, Pearson Education, 2008.
2. 'Programming for Embedded Systems', Dream Tech Software Team, John Wiley, India Pvt. Ltd., 2008.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
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Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Recognize and classify real-time systems	L2
CO2	Apply software development process to a given RTOS application	L2
CO3	Design a given RTOS based application	L3
CO4	Ability to use commercial tools to develop RTOS based applications	L3

Simulation, Modelling and Analysis			
Course Code	22LEL245	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	2:0:2	SEE Marks	50
Total Hours of Pedagogy	25 Hours of teaching and 10-12 sessions for Skill Development Activities	Total Marks	100
Credits	3	Exam Hours	03

Course Learning objectives: Thiscoursewillenablestudentsto:

- Define the basics of simulation modelling and replicating the practical situations in organizations
- Generate random numbers and random variates using different techniques.
- Develop simulation model using heuristic methods.
- Analysis of Simulation models using input analyzer, and output analyzer.
- Explain Verification and Validation of simulation model.

Module-1

Basic Simulation Modeling:Nature of simulation, Systems, Models and Simulation, Discrete- Event Simulation, Simulation of Single Server Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high-level architecture, Steps in sound simulation study, and other types of simulation, Advantages and disadvantages.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-2

Review of Basic Probability and Statistics: Random Variables and their properties, SimulationOutput Data and Stochastic Processes, Estimationof Means, Variances and Correlations, ConfidenceIntervals and Hypothesis tests for the Mean**.**

Building valid, credible and appropriately detailed simulation models: Introduction and definitions, Guidelines for determining the level of model's detail, Management's Role in the Simulation Process, Techniques for increasing model validity and credibility, Statistical procedure for comparing the real-world observations and simulation output data.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-3

Selecting Input Probability Distributions: Useful probability distributions, activity I, II andIII. Shifted and truncated distributions; Specifyingmultivariate distribution, correlations, andstochastic processes; Selecting the distribution in the absence of data, Models of arrival process**.**

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-4

Random Number Generators: Linear congruential Generators, Other kinds, Testing number generators,

Generating the Random Variates: General approaches, generating continuous random variates, generating discrete random variates, generating random vectors, and correlated random variates; Generating arrival processes.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Module-5

Output data analysis for a single system: Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis; Statistical analysis for terminating simulation; Statistical analysis for steady state parameters; Statistical analysis for steady state cycle parameters; Multiple measures of performance, Time plots of important variables.

Teaching-Learning Process	Chalk and talk method / PowerPoint Presentations

Assessment Details (both CIE and SEE)

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Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
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to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Averill Law, "Simulation modeling and analysis", McGraw Hill 4th edition, 2007.

Reference Books:

2. TayfurAltiok and Benjamin Melamed, "Simulation modeling and analysis with ARENA", Elsevier, Academic press, 2007.
3. Jerry Banks, "Discrete event system Simulation", Pearson, 2009
4. Seila Ceric and Tadikamalla, "Applied simulation modeling", Cengage, 2009.
5. George. S. Fishman, "Discrete event simulation", Springer, 2001.
6. Frank L. Severance, "System modeling and simulation", Wiley, 2009..

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
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Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Describe the role of important elements of discrete event simulation and modeling paradigm	L2
CO2	Conceptualize real world situations related to systems development decisions, originating from source requirements and goals.	L4
CO3	Develop skills to apply simulation software to construct and execute goal-driven system models.	L4
CO4	Interpret the model and apply the results to resolve critical issues in a real world environment.	L3

Advanced Communication Lab			
Course Code	22LELL26	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	1:2:0	SEE Marks	50
Total Hours of Pedagogy	13 Hours of teaching and 10-13 Practical sessions	Total Marks	100
Credits	2	Exam Hours	03

PartA: EDA Using Cadence OrCAD or OrCAD Lite or any EDA Tool,designandverifythefollowing:

Sl. No.	Experiments
1	SimulationofASKmodulationanddemodulation
2	SimulationofFSKmodulationand demodulation
3	SimulationofBPSKmodulationand demodulation
4	SimulationofQPSKmodulationand demodulation
5	SimulationofsignalconstellationQPSKwithRayleigh fadingandAWGN
6	SimulationofsignalconstellationM-aryQAMwith AWGN fading
7	Tosimulatethecommunicationlink
8	TosimulateZeroForcingalgorithm
9	Tosimulate LMSalgorithm
10	Generationof m-Sequence and verifyits properties
11	GenerationGold Sequenceand verifyitsproperties

ConductofPracticalExamination:

1. Alllaboratoryexperiments areto beincludedforpracticalexamination.
2. Studentsareallowed topickoneexperiment fromthe lot.
3. Strictlyfollowtheinstructionsasprintedon thecoverpageofanswerscript forbreakup ofmarks.
4. Changeofexperiment is allowedonlyonce and Marksallotted totheprocedureparttobemadezero.

AssessmentDetails(bothCIEandSEE)

TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Theminimumpassingmarkforthe CIEis 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has tosecure50% maximum marks ofthe course.

ContinuousInternalEvaluation(CIE):

CIEmarksforthepracticalcourseis **50Marks**.

Thesplit-upofCIEmarksfor record/journalandtest arein theratio **60:40**.

1. Eachexperimenttobeevaluatedforconductionwithobservationsheetandrecordwrite-up.Rubricsfortheevaluationofthejournal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known tostudentsatthebeginning ofthe practical session.
2. Recordshouldcontainallthespecified experimentsinthesyllabusandeachexperimentwrite-upwillbeevaluated for10marks.
3. Totalmarksscoredbythestudentsare scaled downedto30marks(60%ofmaximummarks).
4. Weightageto begivenforneatnessandsubmission ofrecord/write-upontime.
5. Departmentshallconduct02testsfor100marks,thefirsttestshallbeconductedafterthe8thweekofthesemesterandthesecondt estshall be conducted after the 14th weekofthe semester.
6. Ineachtest,testwrite-up,conductionofexperiment,acceptableresult,andproceduralknowledgewillcarryaweightageof60%andtherest 40% for viva-voce.
7. Thesuitablerubricscan bedesignedtoevaluateeach studentsperformanceand learningability.
8. Theaverageof02 tests isscaleddown to**20marks**(40%ofthemaximummarks).

TheSumof**scaled-down**marks scored inthereport write-up/journal and average marksoftwo testsis thetotal CIE marksscoredbythe student.

SemesterEndEvaluation(SEE):

9. SEEmarksfor thepracticalcourseis50Marks.
10. SEEshallbeconducted jointlybythetwo examiners ofthesameinstitute, examinersareappointedbytheUniversity.
11. Alllaboratoryexperimentsaretobeincludedforpractical examination.
12. (Rubrics)Breakupofmarksandtheinstructionsprintedonthecoverpageoftheanswerscripttobestrictlyadheredtobytheexaminers. **OR**based onthecourserequirementevaluation rubricsshallbedecided jointlybyexaminers.
13. Students canpickonequestion (experiment) fromthe questionslotpreparedbytheinternal/externalexaminers jointly.
14. Evaluationoftestwrite-up/conduction procedureandresult/vivawill beconducted jointlybyexaminers.
15. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% ofmaximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, basedon course type, rubrics shallbedecidedbythe examiners)
16. Changeofexperimentisallowed onlyonceand 10%Marksallottedtotheprocedure partto bemadezero.

ThedurationofSEEis03 hours

Suggested ONLINE courses

Sl. No.	Course code	Course Title	National Coordinator	Instructor
1	22AUD27	Introduction To Internet Of Things (12 Weeks)	NPTEL	Prof. Sudip Misra IIT Kharagpur
2		Basics of software defined Radios (4 Weeks)	NPTEL	Prof. Meenakshi Rawat IIT Roorkee
3		Principles of Signal Estimation for MIMO/ OFDM Wireless Communication (12 Weeks)	NPTEL	Prof. Aditya K. Jagannatham IIT Kanpur
4		Programming In Java (12 Weeks)	NPTEL	Prof. DebasisSamanta IIT Kharagpur
5		Fiber Optic Communication Technology (12 Weeks)	NPTEL	Prof. Deepa Venkatesh IIT Madras
6		Introduction to Wireless and Cellular Communications (12 Weeks)	NPTEL	Prof. R. David Koilpillai IIT Madras
7		Introduction to Computer and Network Performance Analysis using Queuing Systems (4 Weeks)	NPTEL	Prof. Varsha Apte IIT Bombay
8		LaTeX &XFig - typesetting software (06 Weeks)	AICTE	Prof Kannan Moudgalya, Principal Investigator of Spoken Tutorial Project Indian Institute of Technology Bombay